

Compal Confidential

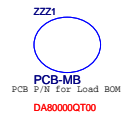
QCL40 MB Schematic Document

LA-8224P

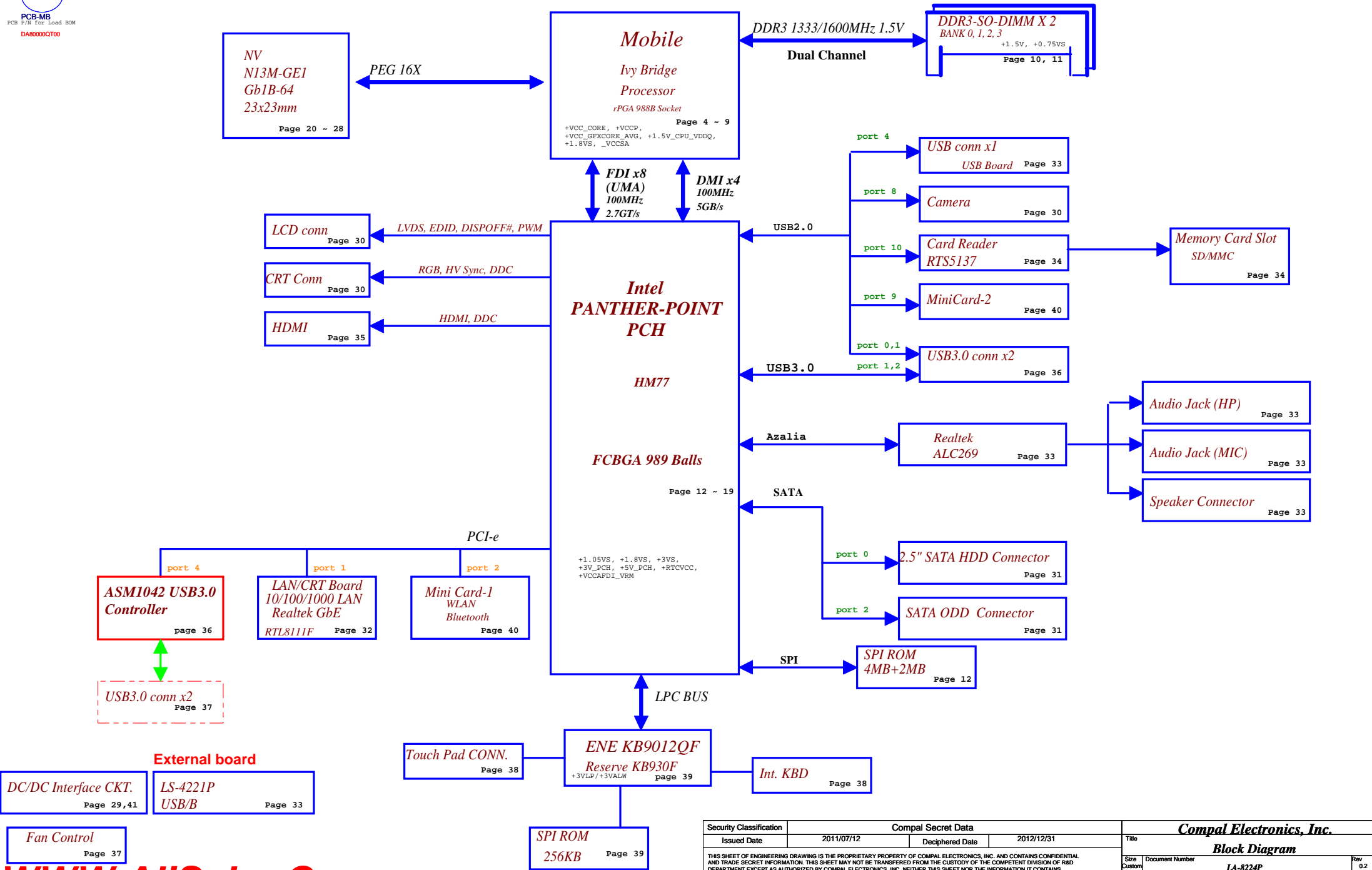
Rev: 0.2

2011.09.28

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				Size	Rev
				Custort	0.2
				LA-8224P	
				Date:	Thursday, October 27, 2011
				Sheet	1 of 59

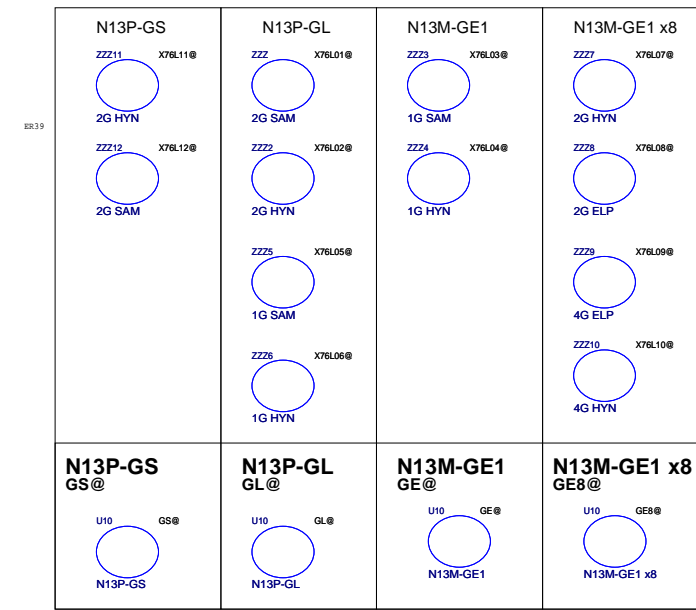


QCL40



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				LA-8224P	
				Date	Thursday, October 27, 2011
				Sheet	2 of 59
				Rev	02

X76@: VRAMX16X8 VRAMX16X4 VRAMX8X8



DIS@: VGA componet
GE8@: N13M-GE1_GB1b

9012@: EC(ENE 9012 chip)
930@: EC(ENE 930 chip)
XDP@: Intel debug port

IU3@: USB3.0 by PCH
USB30@:USB3.0 controller IC

AI@: AI Charger
NAI@: Non AI Charger

SMBUS Control Table							
	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :



: means Digital Ground



: means Analog Ground

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

Voltage Rails

Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 510N power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

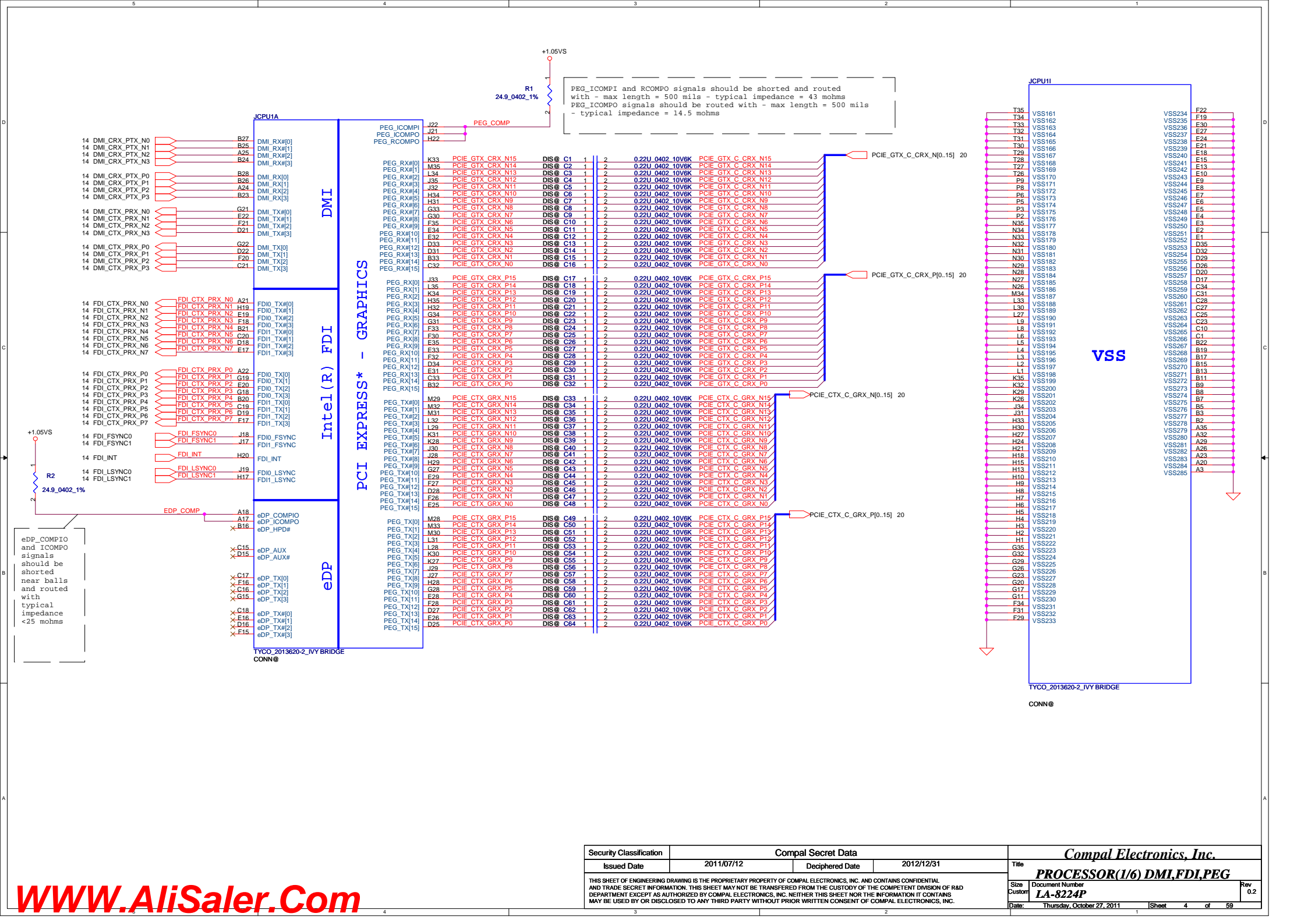
SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

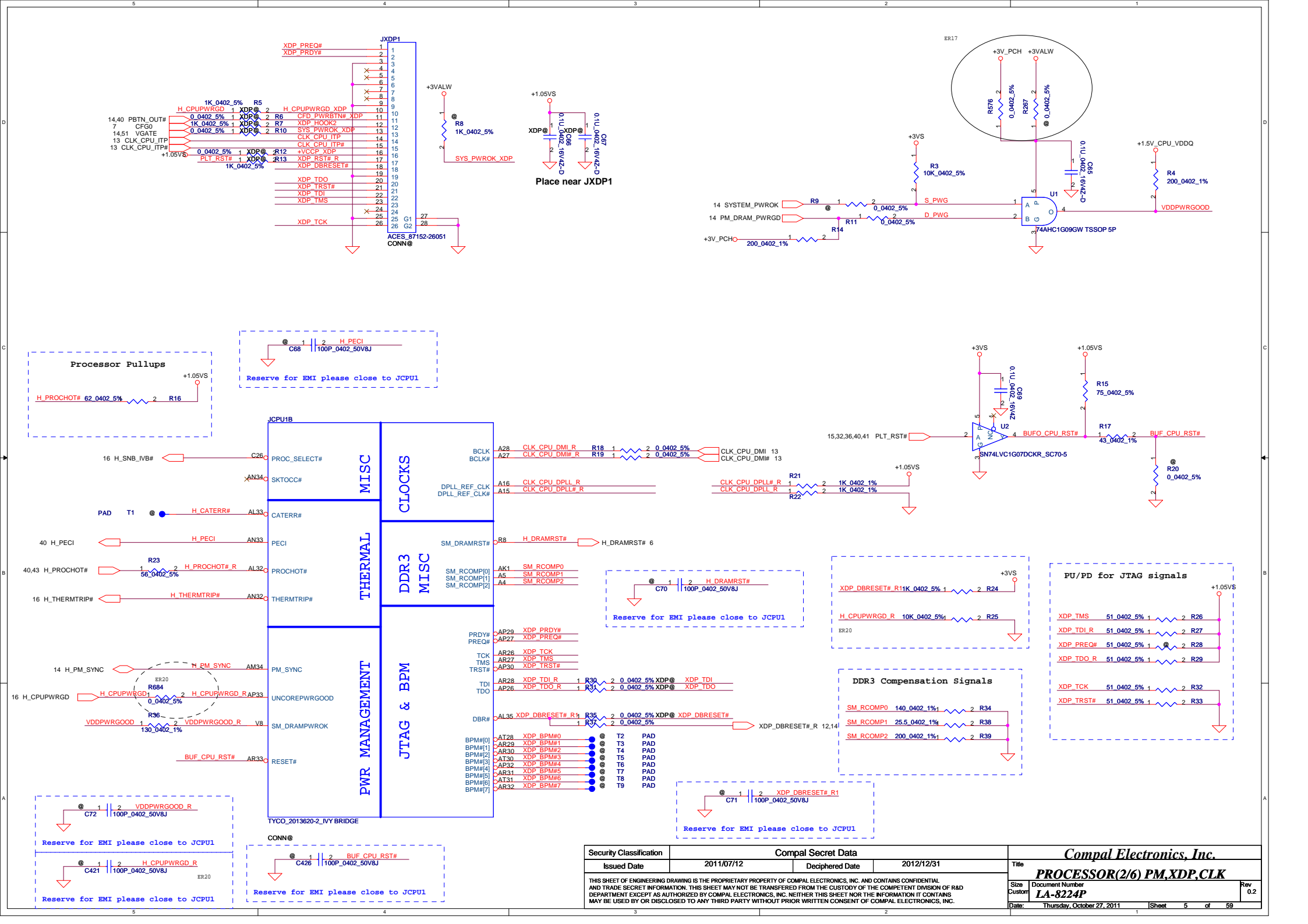
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				Date:	Thursday, October 27, 2011
				Sheet	3 of 59
				Rev	0.2

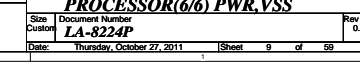
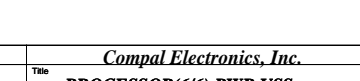
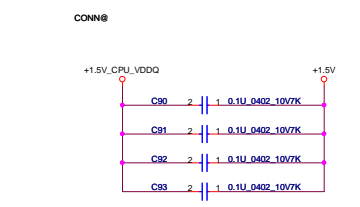
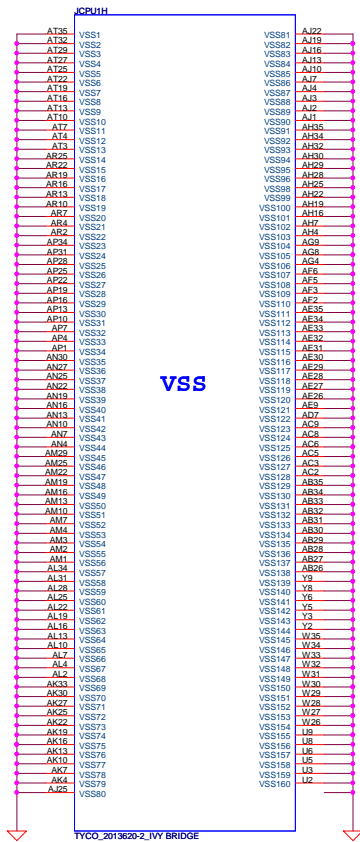
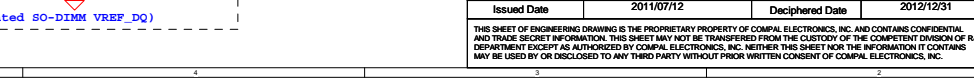
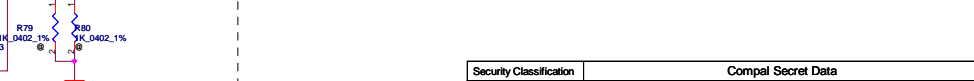
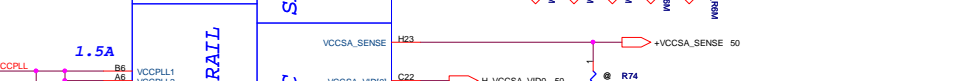
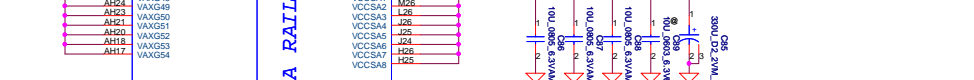
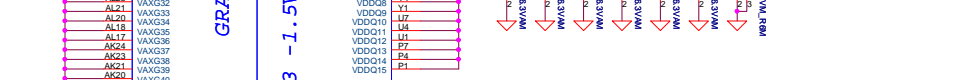
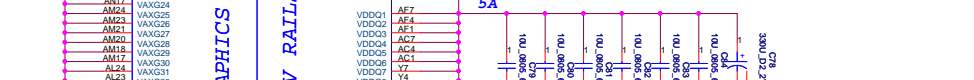
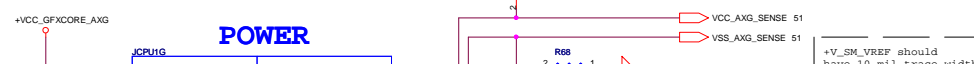
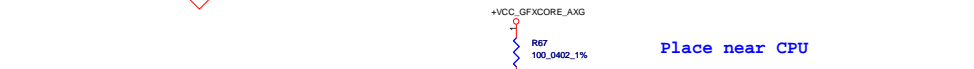
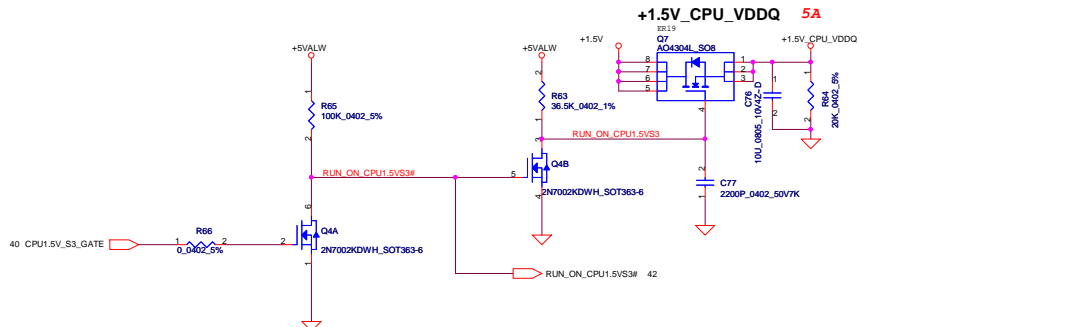
PCH	USB3 PORT	DESTINATION
	1	USB2.0+3.0
	2	USB2.0+3.0
	3	None
	4	None

PCH	USB2 PORT	DESTINATION
	0	USB2.0+3.0
	1	USB2.0+3.0
	2	None
	3	None
	4	JMINI1 (WLAN) Bluetooth
	5	None
	6	None
	7	None
	8	CAMERA
	9	USB2
	10	Card Reader
	11	None
	12	None
	13	None

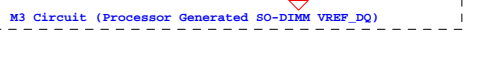
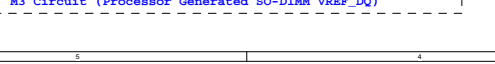
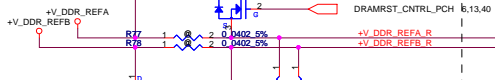
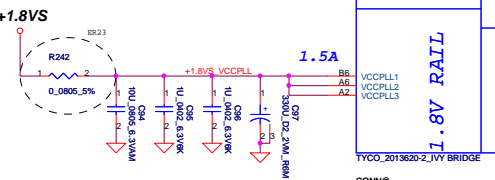
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	USB3.0 controller
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

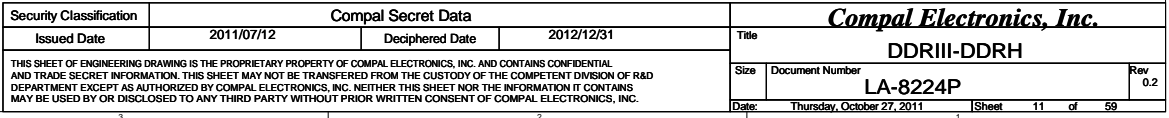




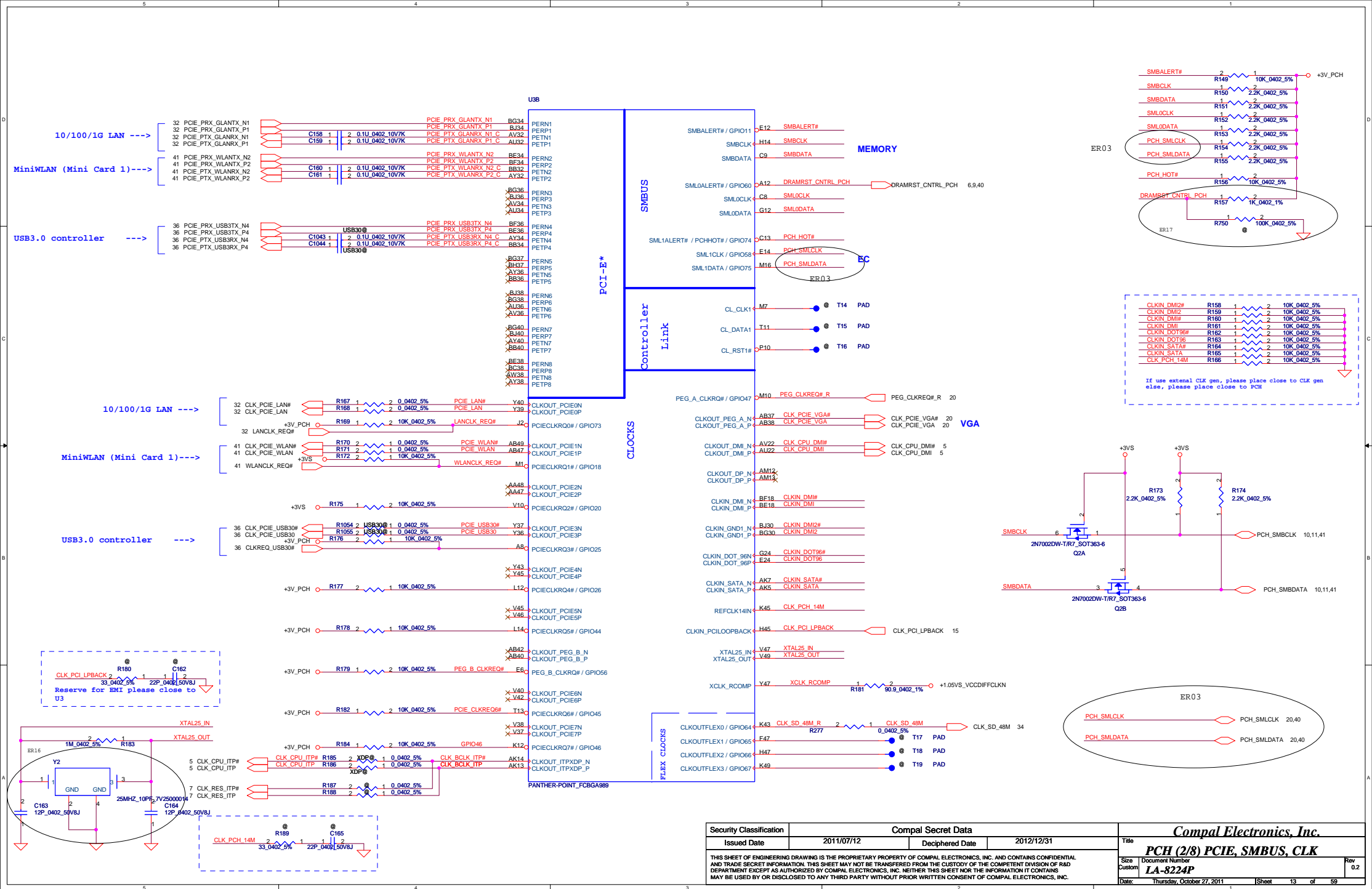


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Size	Customer	Document Number	1A-8224P	Date	Thursday, October 27, 2011	Sheet 9 of 59

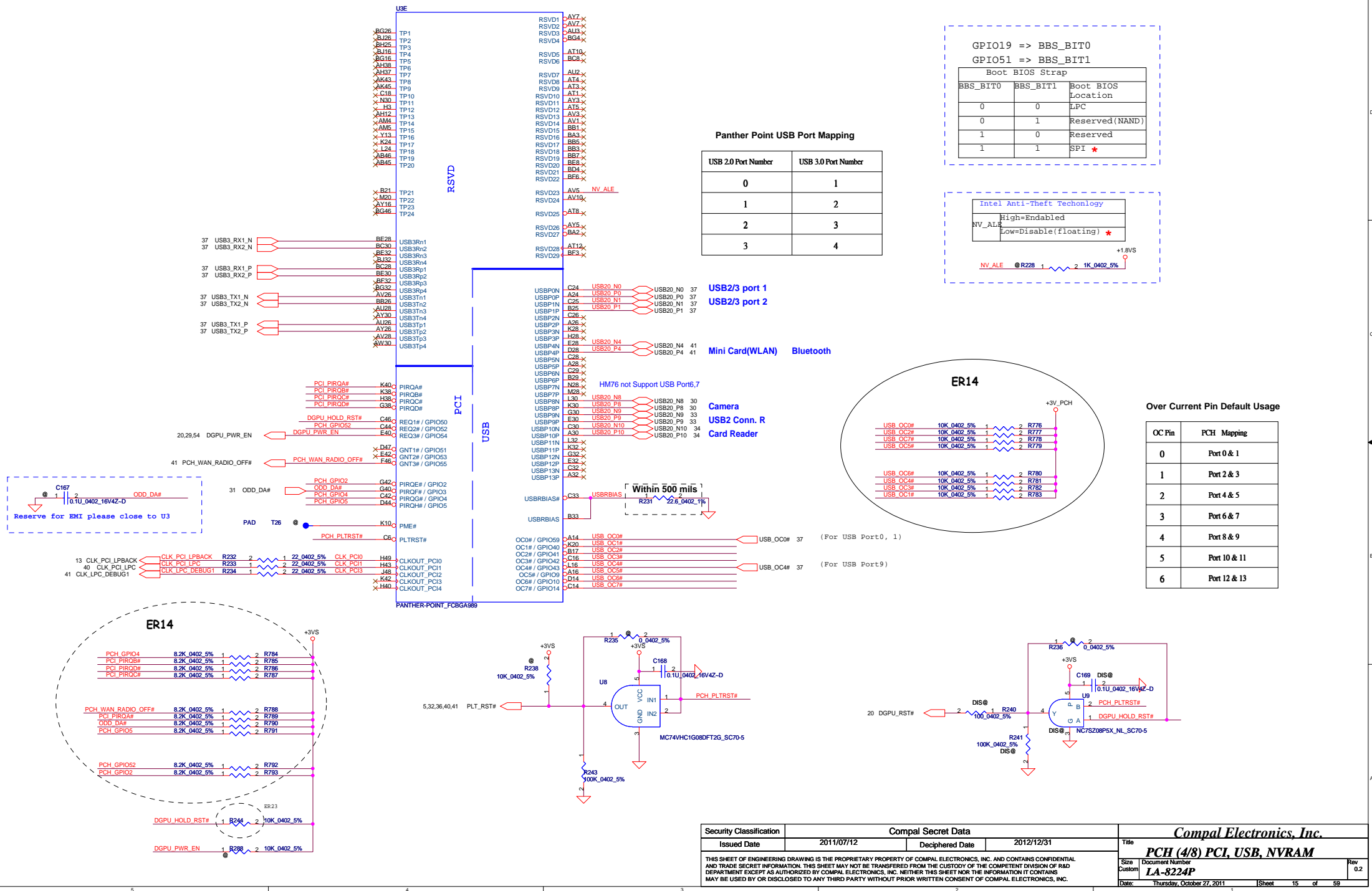








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				Custom	0.2
				Document Number LA-8224P	
Date:	Thursday, October 27, 2011	Sheet	13	of	59



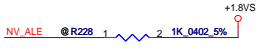
Panther Point USB Port Mapping

USB 2.0 Port Number	USB 3.0 Port Number
0	1
1	2
2	3
3	4

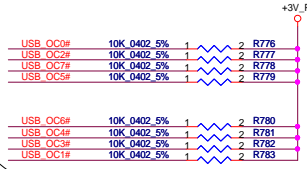
GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap		
BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPI *

Intel Anti-Theft Technology	
NV_ALE	High=Enabled Low=Disable(floating) *

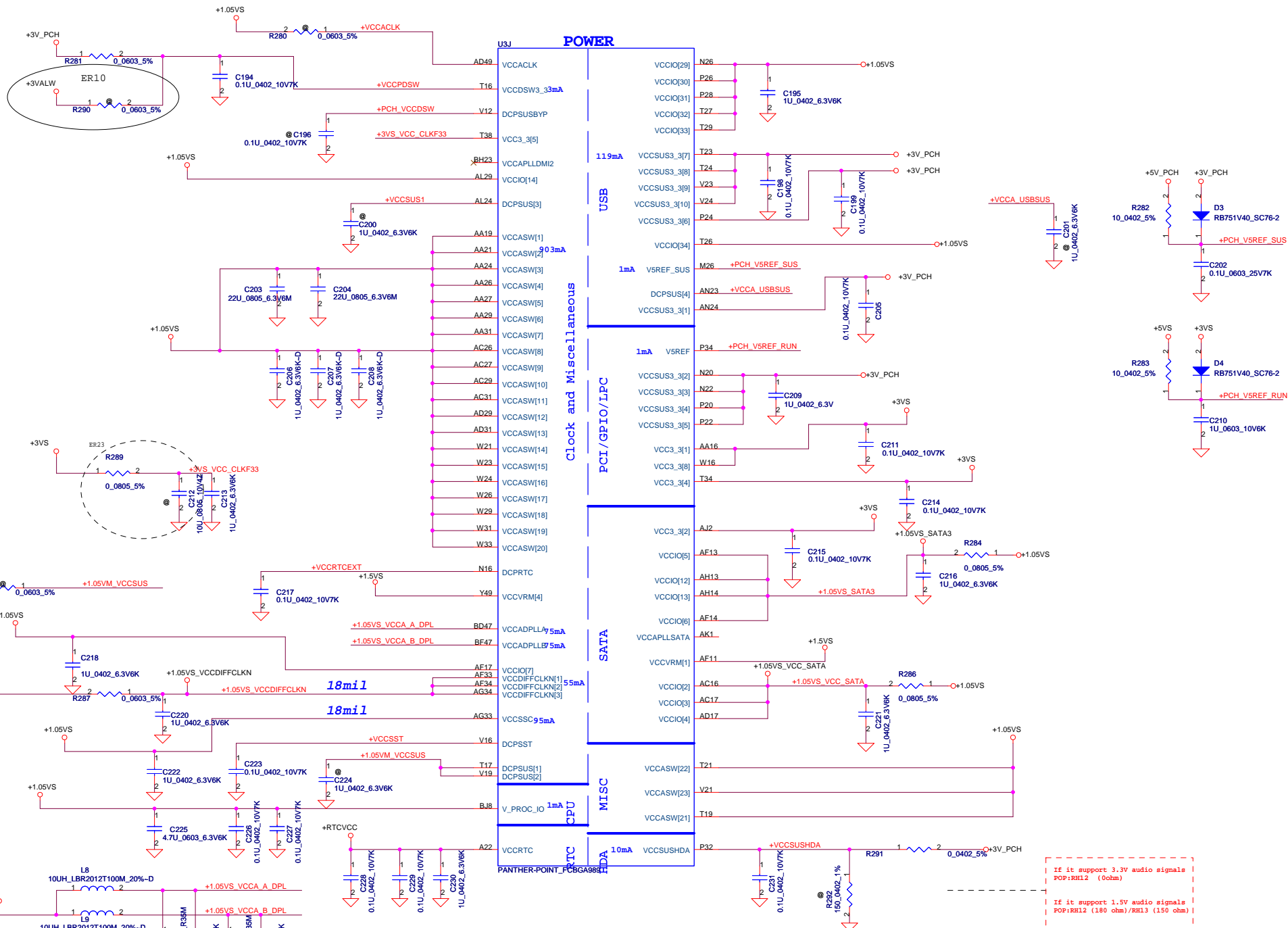


ER14



Over Current Pin Default Usage

OC Pin	PCH Mapping
0	Port 0 & 1
1	Port 2 & 3
2	Port 4 & 5
3	Port 6 & 7
4	Port 8 & 9
5	Port 10 & 11
6	Port 12 & 13



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Size	Custom	Document Number	LA-8224P	Rev	0.2
Date:	Thursday, October 27, 2011	Sheet	18	of	59

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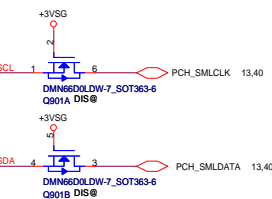
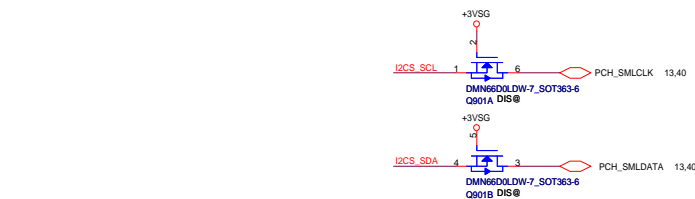
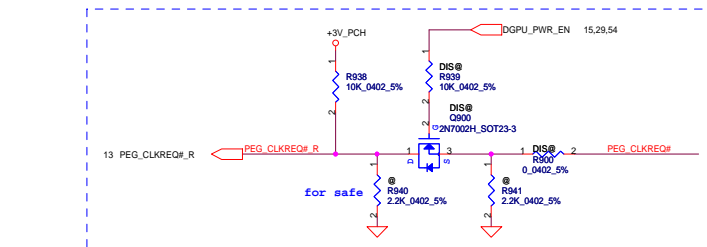
U3H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK42
AA33	VSS[4]	VSS[83] AK46
AA34	VSS[5]	VSS[84] AK6
AB11	VSS[6]	VSS[85] AL16
AB14	VSS[7]	VSS[86] AL17
AB39	VSS[8]	VSS[87] AL19
AB4	VSS[9]	VSS[88] AL2
AB43	VSS[10]	VSS[89] AL21
AB5	VSS[11]	VSS[90] AL23
AB7	VSS[12]	VSS[91] AL26
AC19	VSS[13]	VSS[92] AL27
AC2	VSS[14]	VSS[93] AL31
AC21	VSS[15]	VSS[94] AL33
AC24	VSS[16]	VSS[95] AL34
AC33	VSS[17]	VSS[96] AL48
AC34	VSS[18]	VSS[97] AM11
AC48	VSS[19]	VSS[98] AM14
AD10	VSS[20]	VSS[99] AM36
AD11	VSS[21]	VSS[100] AM39
AD12	VSS[22]	VSS[101] AM43
AD13	VSS[23]	VSS[102] AM45
AD19	VSS[24]	VSS[103] AM46
AD24	VSS[25]	VSS[104] AM7
AD26	VSS[26]	VSS[105] AN2
AD27	VSS[27]	VSS[106] AN29
AD33	VSS[28]	VSS[107] AN3
AD34	VSS[29]	VSS[108] AN31
AD36	VSS[30]	VSS[109] AP12
AD37	VSS[31]	VSS[110] AP19
AD38	VSS[32]	VSS[111] AP28
AD39	VSS[33]	VSS[112] AP30
AD4	VSS[34]	VSS[113] AP32
AD40	VSS[35]	VSS[114] AP38
AD42	VSS[36]	VSS[115] AP4
AD43	VSS[37]	VSS[116] AP42
AD45	VSS[38]	VSS[117] AP46
AD46	VSS[39]	VSS[118] AP6
AD8	VSS[40]	VSS[119] AR2
AE2	VSS[41]	VSS[120] AR48
AE3	VSS[42]	VSS[121] AT11
AE10	VSS[43]	VSS[122] AT13
AE12	VSS[44]	VSS[123] AT18
AD14	VSS[45]	VSS[124] AT22
AD16	VSS[46]	VSS[125] AT26
AE16	VSS[47]	VSS[126] AT28
AE19	VSS[48]	VSS[127] AT30
AE24	VSS[49]	VSS[128] AT32
AE26	VSS[50]	VSS[129] AT34
AE27	VSS[51]	VSS[130] AT39
AE29	VSS[52]	VSS[131] AT42
AF31	VSS[53]	VSS[132] AT46
AF38	VSS[54]	VSS[133] AT7
AF4	VSS[55]	VSS[134] AU24
AF42	VSS[56]	VSS[135] AU30
AF46	VSS[57]	VSS[136] AV16
AF5	VSS[58]	VSS[137] AV20
AF7	VSS[59]	VSS[138] AV24
AF8	VSS[60]	VSS[139] AV30
AG19	VSS[61]	VSS[140] AV38
AG2	VSS[62]	VSS[141] AV4
AG31	VSS[63]	VSS[142] AV43
AG48	VSS[64]	VSS[143] AV8
AH11	VSS[65]	VSS[144] AW14
AH3	VSS[66]	VSS[145] AW18
AH36	VSS[67]	VSS[146] AW2
AH39	VSS[68]	VSS[147] AW22
AH40	VSS[69]	VSS[148] AW26
AH42	VSS[70]	VSS[149] AW28
AH46	VSS[71]	VSS[150] AW32
AH7	VSS[72]	VSS[151] AW34
AJ19	VSS[73]	VSS[152] AW38
AJ21	VSS[74]	VSS[153] AW40
AJ24	VSS[75]	VSS[154] AW48
AJ33	VSS[76]	VSS[155] AV11
AJ34	VSS[77]	VSS[156] AY12
AK12	VSS[78]	VSS[157] AY22
AK3	VSS[79]	VSS[158] AY28

PANTHER-POINT_FCBGA989

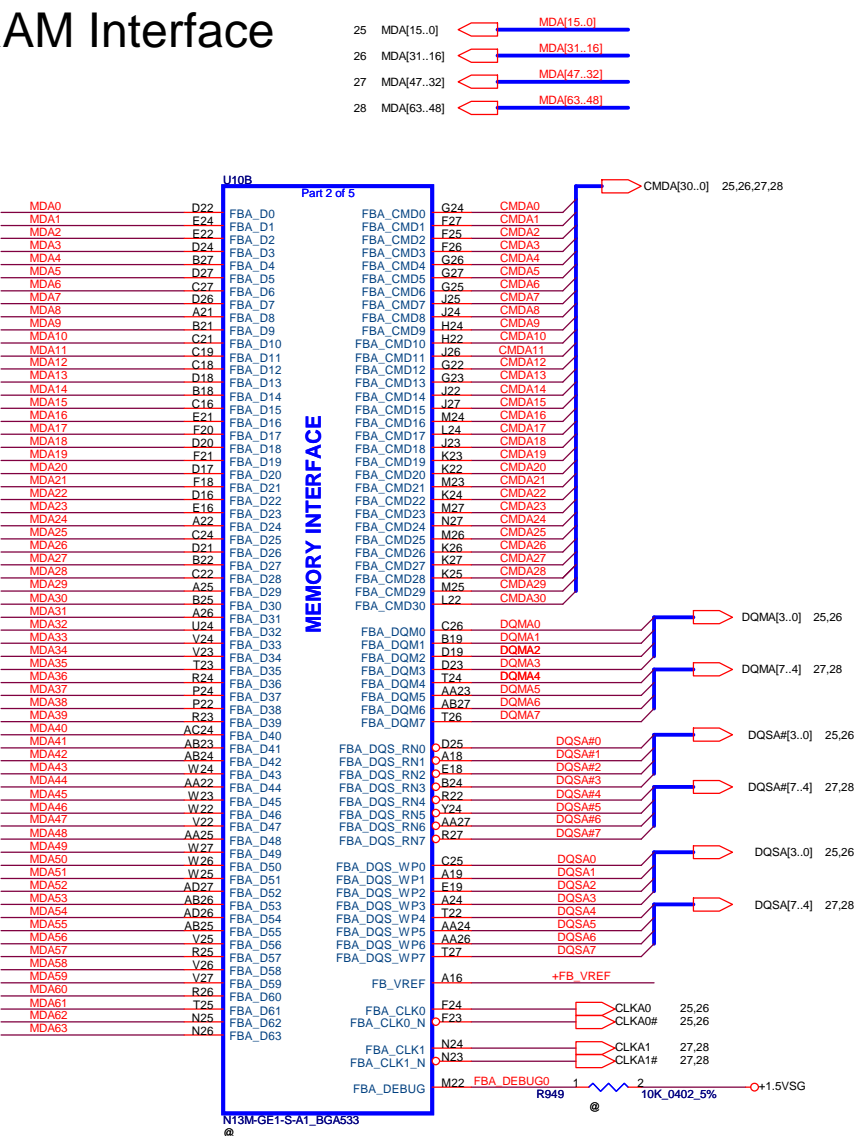
U3I		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B35	VSS[169]	VSS[269] L28
B39	VSS[170]	VSS[270] L36
B7	VSS[171]	VSS[271] L48
F45	VSS[172]	VSS[272] M12
BB12	VSS[173]	VSS[273] P16
BB16	VSS[174]	VSS[274] M18
BB20	VSS[175]	VSS[275] M22
BB22	VSS[176]	VSS[276] M24
BB24	VSS[177]	VSS[277] M30
BB28	VSS[178]	VSS[278] M32
BB30	VSS[179]	VSS[279] M34
BB38	VSS[180]	VSS[280] M38
BB4	VSS[181]	VSS[281] M4
BB46	VSS[182]	VSS[282] M42
BC14	VSS[183]	VSS[283] M46
BC18	VSS[184]	VSS[284] M8
BC2	VSS[185]	VSS[285] N18
BC22	VSS[186]	VSS[286] P30
BC26	VSS[187]	VSS[287] N47
BC32	VSS[188]	VSS[288] P11
BC34	VSS[189]	VSS[289] P18
BC36	VSS[190]	VSS[290] T33
BC40	VSS[191]	VSS[291] P40
BC42	VSS[192]	VSS[292] P43
BC48	VSS[193]	VSS[293] P47
BD46	VSS[194]	VSS[294] P7
BD5	VSS[195]	VSS[295] R48
BE22	VSS[196]	VSS[296] T12
BE26	VSS[197]	VSS[297] T31
BE40	VSS[198]	VSS[298] T37
BF10	VSS[199]	VSS[299] T4
BF12	VSS[200]	VSS[300] W34
BF16	VSS[201]	VSS[301] T46
BF20	VSS[202]	VSS[302] T47
BF22	VSS[203]	VSS[303] T8
BF24	VSS[204]	VSS[304] V11
BF26	VSS[205]	VSS[305] V17
BF28	VSS[206]	VSS[306] V26
BD3	VSS[207]	VSS[307] V27
BF30	VSS[208]	VSS[308] V29
BF38	VSS[209]	VSS[309] V31
BF40	VSS[210]	VSS[310] V36
BF8	VSS[211]	VSS[311] V39
BG17	VSS[212]	VSS[312] V43
BG21	VSS[213]	VSS[313] V7
BG33	VSS[214]	VSS[314] W17
BG44	VSS[215]	VSS[315] W19
BG8	VSS[216]	VSS[316] W2
BH11	VSS[217]	VSS[317] W27
BH15	VSS[218]	VSS[318] W48
BH17	VSS[219]	VSS[319] Y12
AU00	VSS[220]	VSS[320] Y38
H10	VSS[221]	VSS[321] Y4
BH27	VSS[222]	VSS[322] Y42
BH31	VSS[223]	VSS[323] Y8
BH33	VSS[224]	VSS[324] BG29
BH35	VSS[225]	VSS[325] N24
BH39	VSS[226]	VSS[326] A33
BH43	VSS[227]	VSS[327] AD47
BH7	VSS[228]	VSS[328] B43
D3	VSS[229]	VSS[329] BG41
D12	VSS[230]	VSS[330] G14
D16	VSS[231]	VSS[331] H16
D18	VSS[232]	VSS[332] T36
D22	VSS[233]	VSS[333] BG22
D24	VSS[234]	VSS[334] BG24
D26	VSS[235]	VSS[335] C22
D30	VSS[236]	VSS[336] AP13
D32	VSS[237]	VSS[337] M14
D34	VSS[238]	VSS[338] AP3
D38	VSS[239]	VSS[339] AP1
D42	VSS[240]	VSS[340] BE16
D8	VSS[241]	VSS[341] BC28
E18	VSS[242]	VSS[342] BJ28
E26	VSS[243]	
G18	VSS[244]	
G20	VSS[245]	
G26	VSS[246]	
G28	VSS[247]	
G36	VSS[248]	
G48	VSS[249]	
H12	VSS[250]	
H18	VSS[251]	
H22	VSS[252]	
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

PANTHER-POINT_FCBGA989

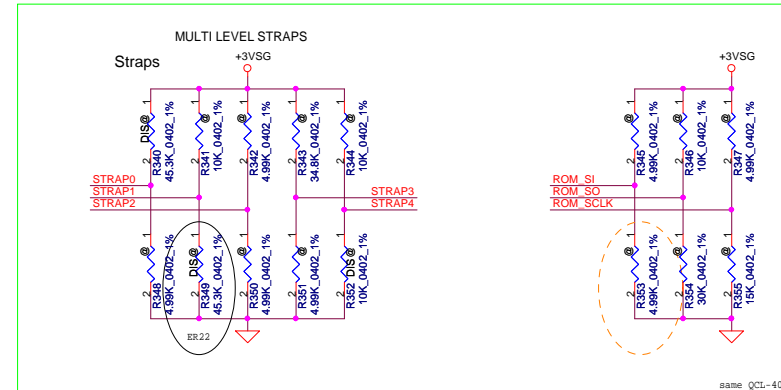
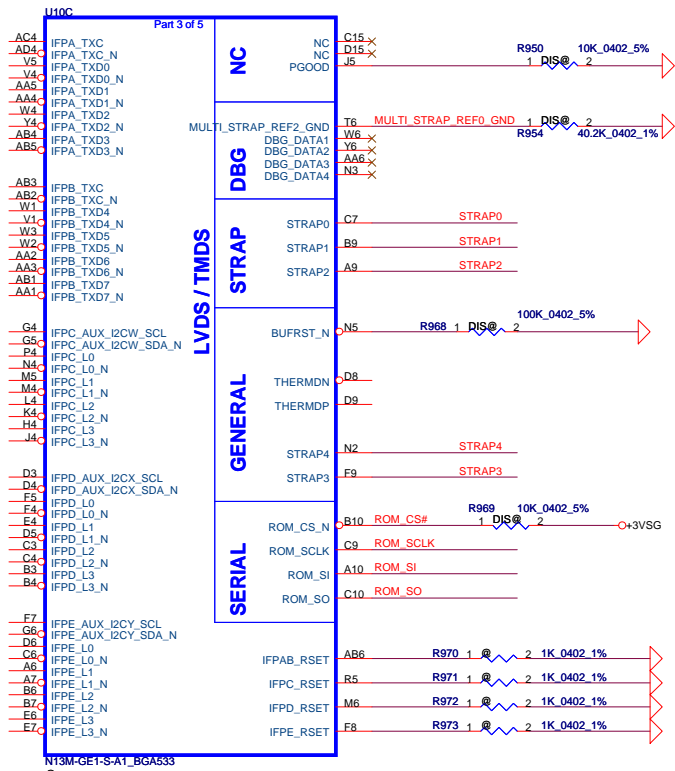
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				Sheet 19	of 59



VRAM Interface



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				Document Number	
				LA-8224P	
				Rev	
				0.2	
				Date	
				Thursday, October 27, 2011	
				Sheet	
				21 of 59	



Need check with NVIDIA

For N13M-GE1 GB1b-64 256Mx8 strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	667+ MHz	256M* 8* 8 2GB	HYNIX SA000056000 H5TQ2G83CFR-H9C	R PH 45K	R PL 45K	R PH 5K	R PL 5K	R PL 10K	R PL 10K	R PL 30K	R PH 5K
N13M-GE1	667+ MHz	256M* 8* 8 2GB	ELPIDA SA000056P00 EDJ2108BCSE-DJ-F	R PH 45K	R PL 45K	R PH 5K	R PL 5K	R PL 10K	R PL 10K	R PL 30K	R PH 5K
N13M-GE1	667+ MHz	512M* 8* 8 4GB	HYNIX SA00005BL00 H5TQ4G83MFR-PBC	R PH 45K	R PL 45K	R PH 5K	R PL 5K	R PL 10K	R PL 15K	R PL 30K	R PH 5K
N13M-GE1	667+ MHz	512M* 8* 8 4GB	ELPIDA SA00005AA00 EDJ4208BBBG-GN-F	R PH 45K	R PL 45K	R PH 5K	R PL 5K	R PL 10K	R PL 20K	R PL 30K	R PH 5K

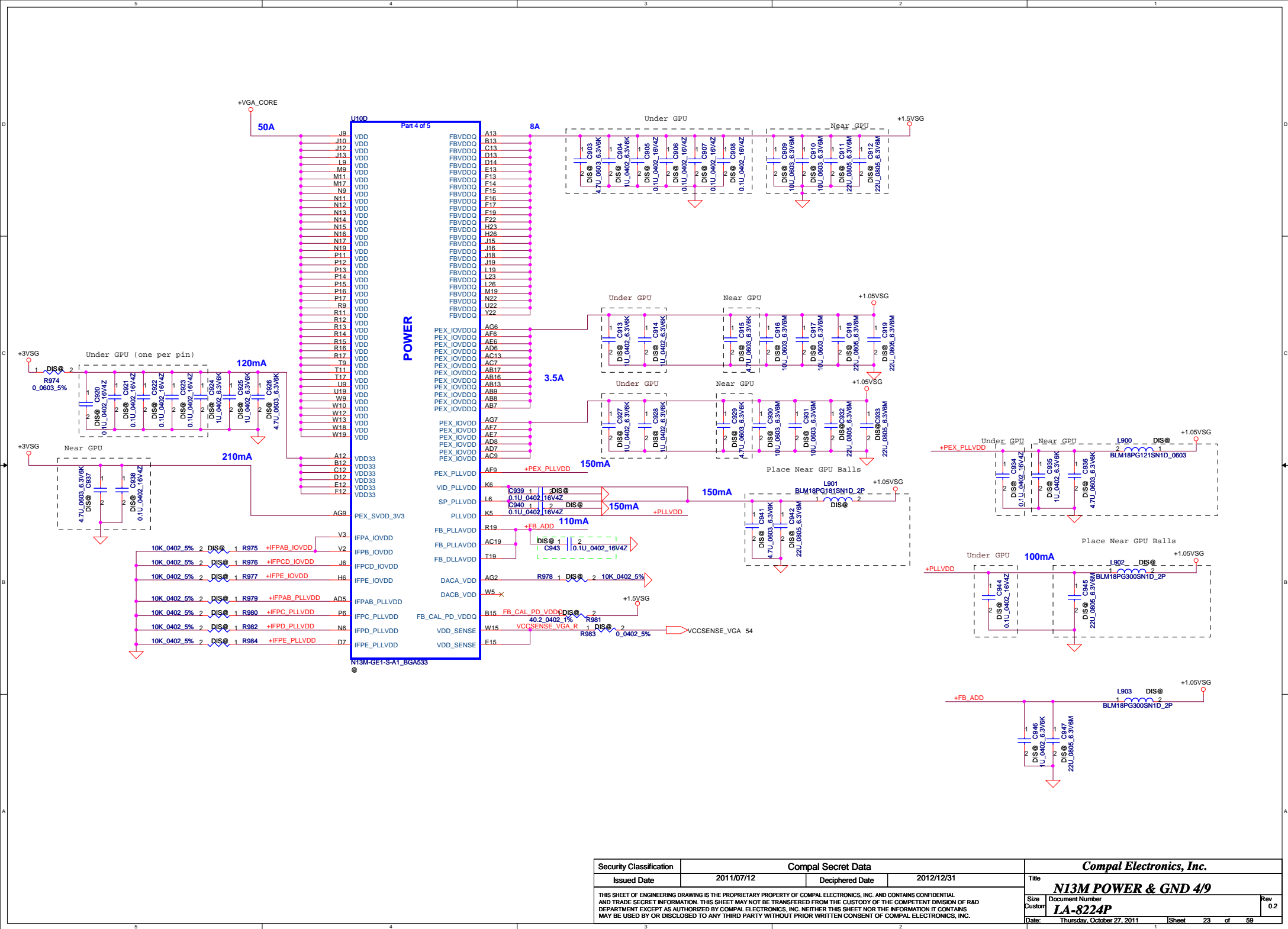
256M*8*8

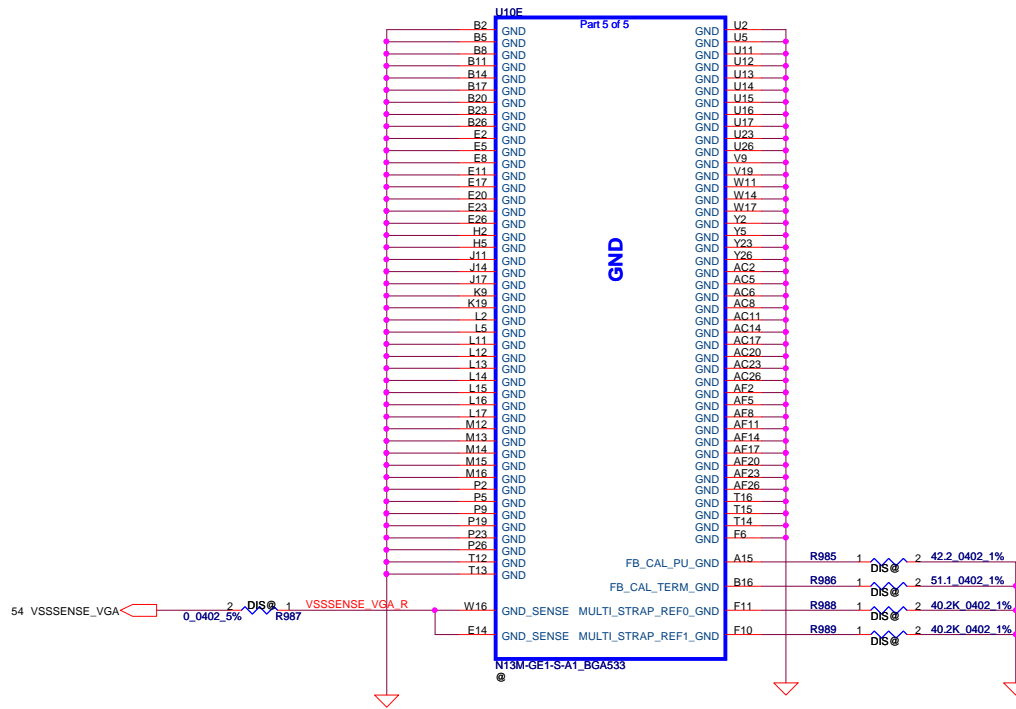
- SA000056000
DDR3 1600 256*8 1.5V FBGA78
HYNIX/H5TQ2G83CFR-PBC
- SA000056P00
DDR3 1600 256*8 1.5V FBGA78
ELPIDA/EDJ2108BDBG-GN-F

512M*8*8

- SA00005BL00
DDR3 1600 512M*8 1.5V FBGA78
HYNIX/H5TQ4G83MFR-PBC
- SA00005AA00
DDR3 1600 512M*8 1.5V FBGA78
ELPIDA/EDJ4208BBBG-GN-F

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				Sheet	22 of 59



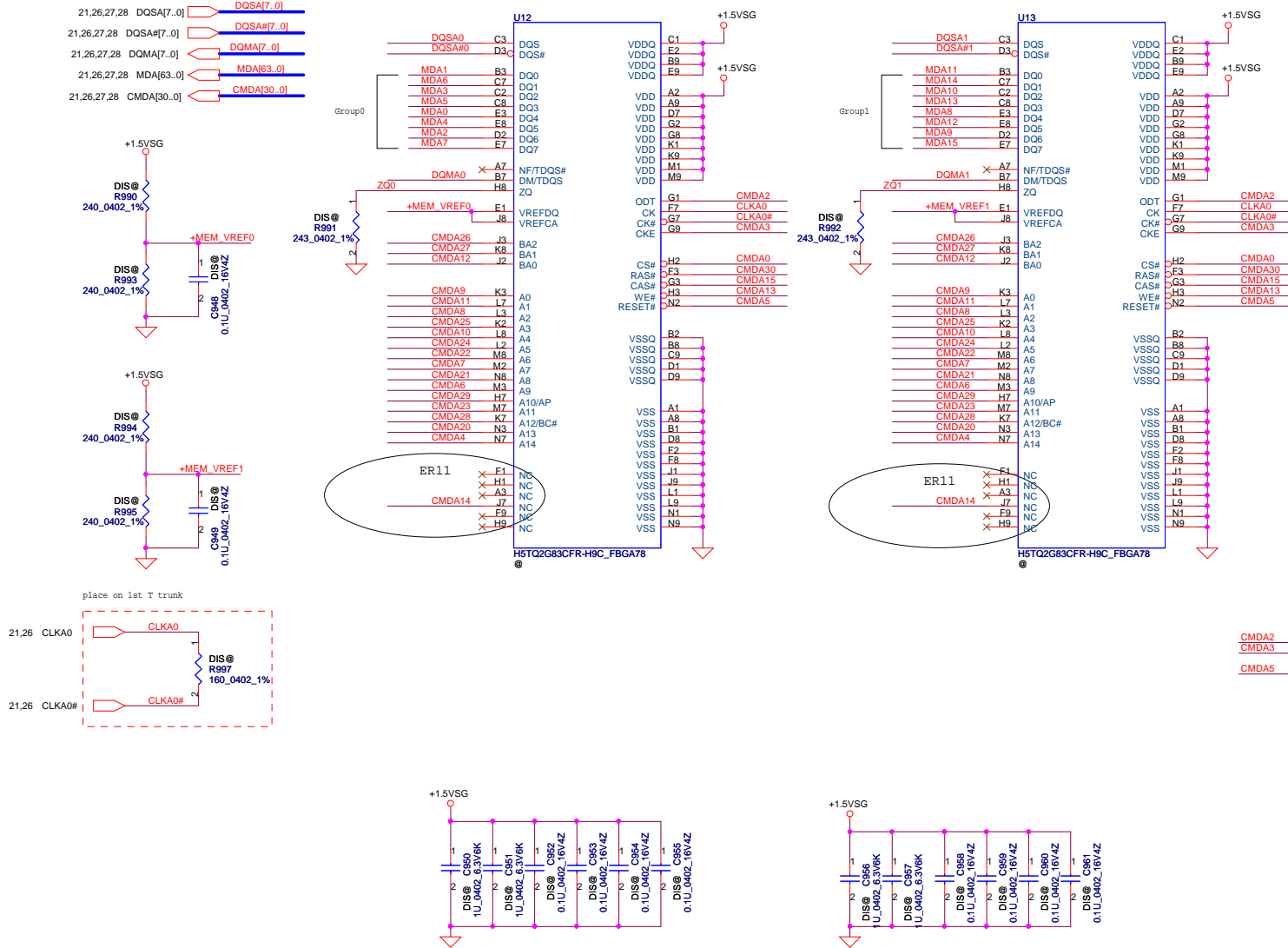


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										N13M POWER & GND 5/9	
										Size	
										Document Number	
										LA-8224P	
										Rev	
										0.2	
										Date	
										Thursday, October 27, 2011	
										Sheet	
										24	
										of	
										59	

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VRAM DDR3 chips

256Mx8 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

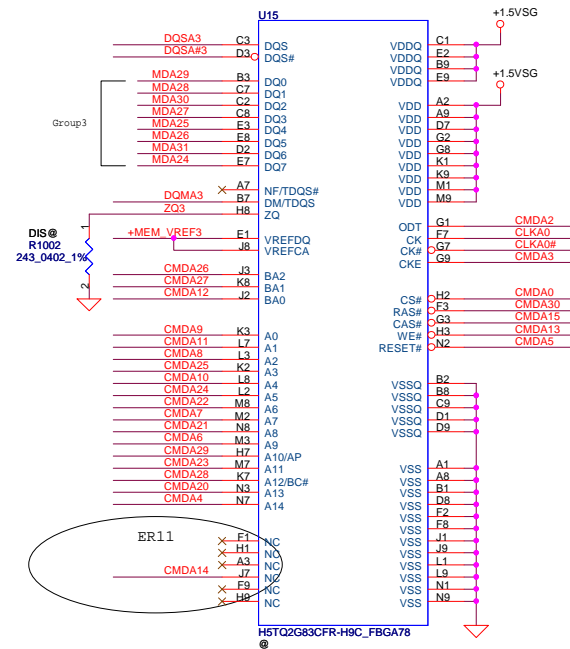
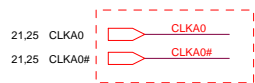
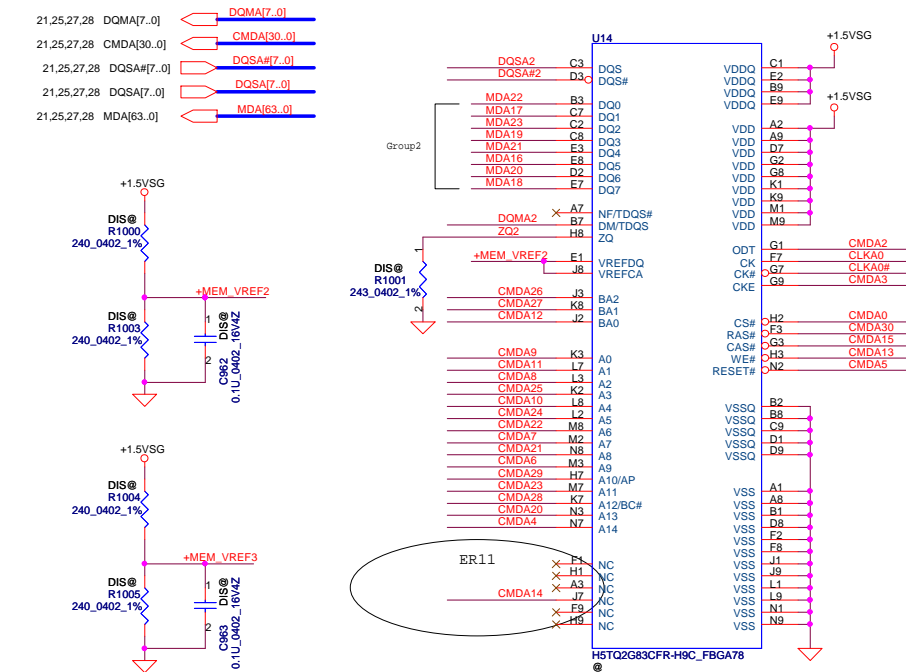
Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA)
Elpida : SAxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxxx)

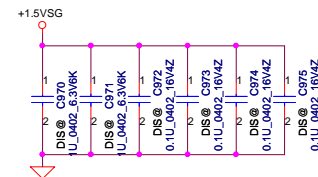
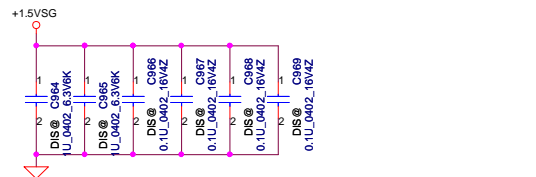
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Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA) Elpida : SAxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxxx)				
Compal Electronics, Inc.				
N13M DDR3 6/9				
Size	Document Number	Rev		
Custom	LA-8224P	0.2		
Date:	Thursday, October 27, 2011	Sheet	25	of 59

VRAM DDR3 chips

256Mx8 DDR3 *8==>2GB



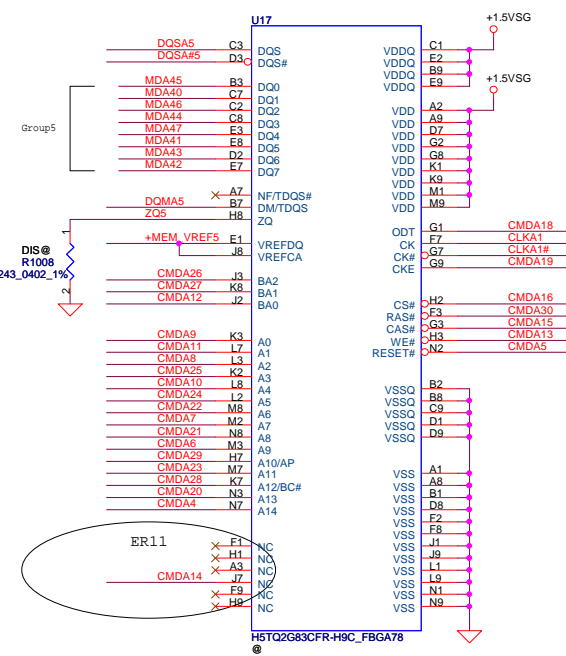
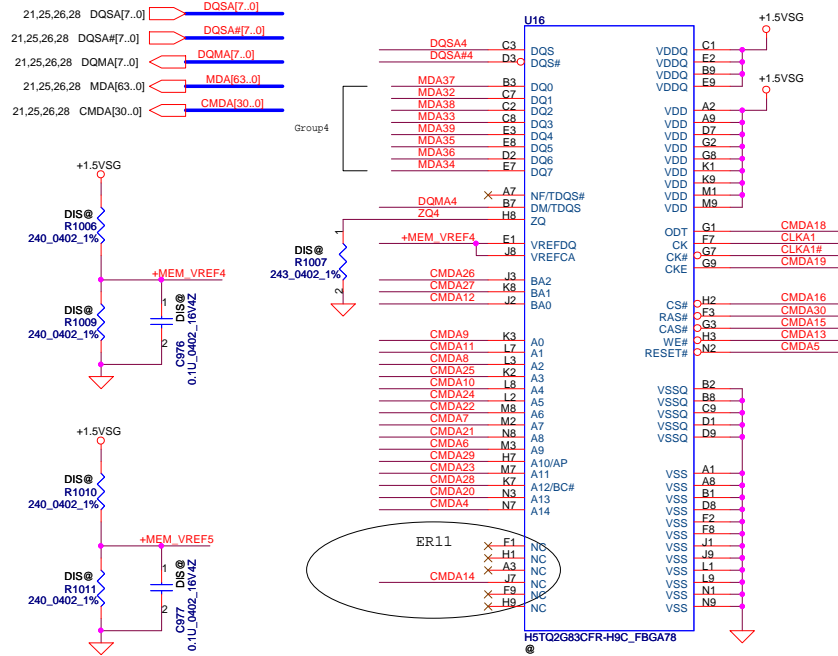
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH



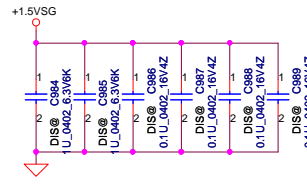
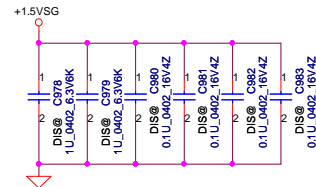
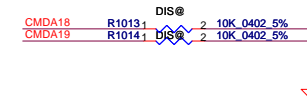
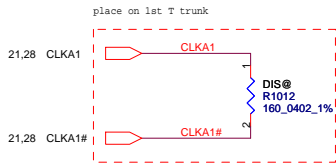
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				LA-8224P		
				Date:	Thursday, October 27, 2011	Sheet 26 of 59

VRAM DDR3 chips

256Mx8 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

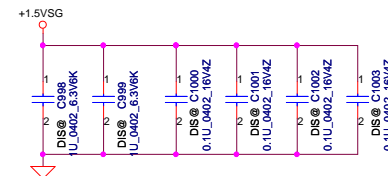
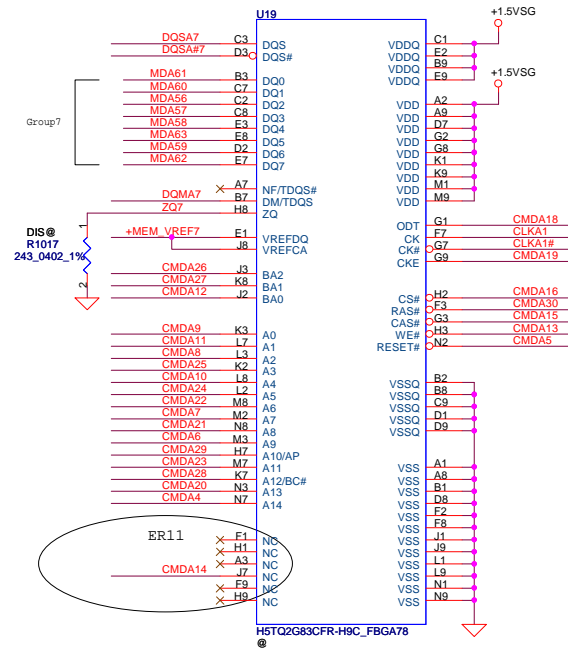
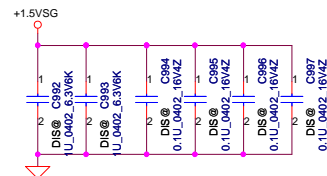
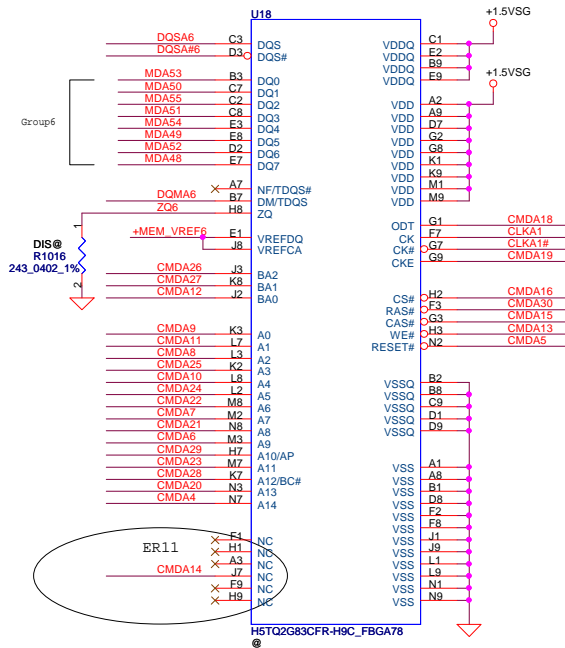
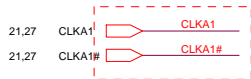
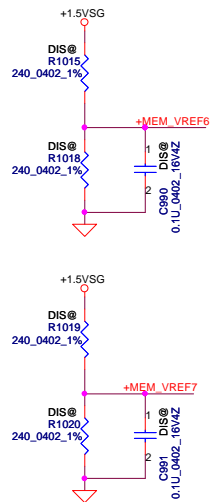
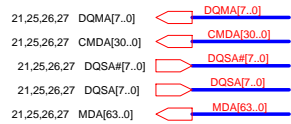


Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA)
Elpida : SAxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxxx)

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		Date Thursday, October 27, 2011	Rev 0.2
		Sheet 27	of 59

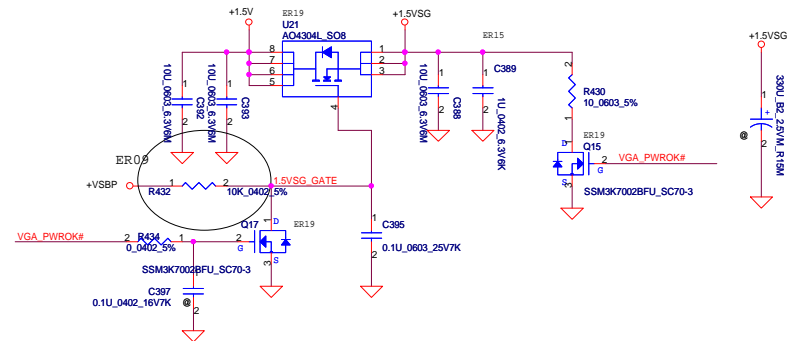
VRAM DDR3 chips

256Mx8 DDR3 *8==>2GB

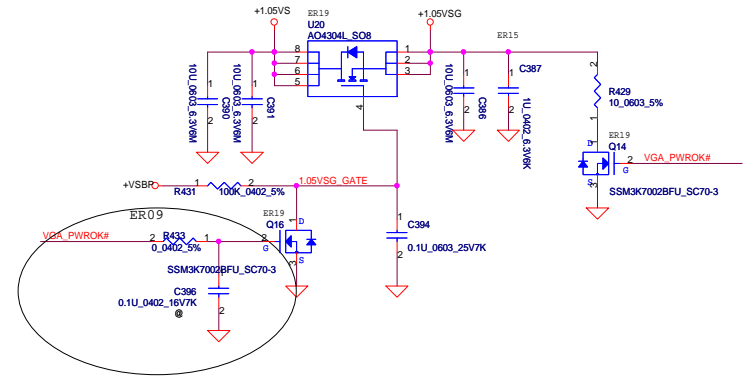


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

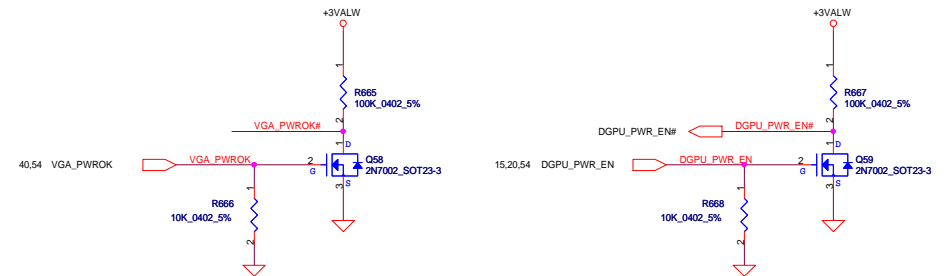
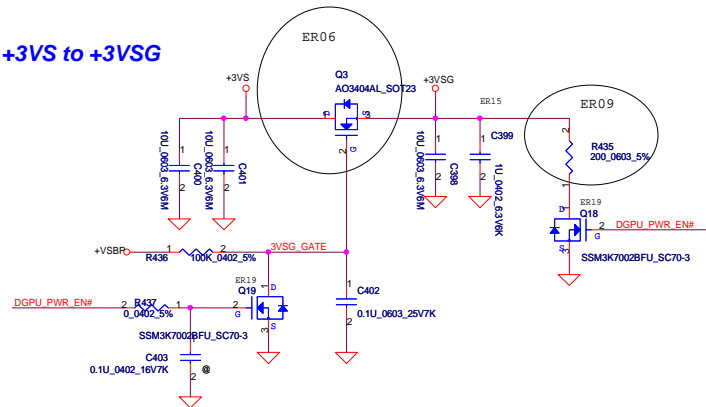
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+VCCP to +1.05VSG

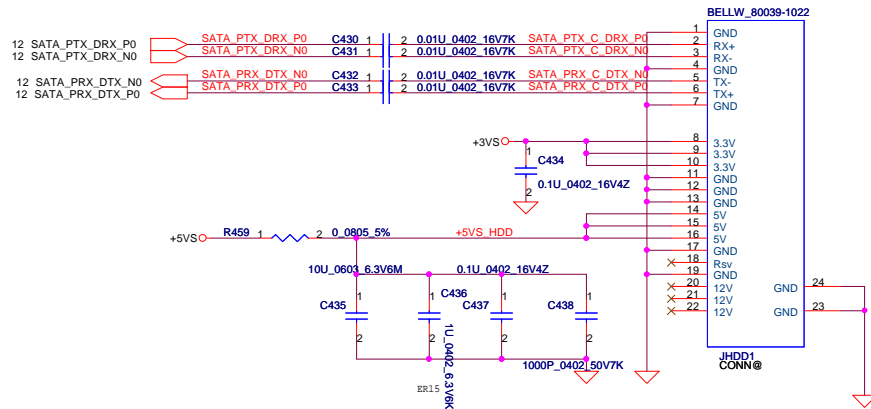


+3VS to +3VSG

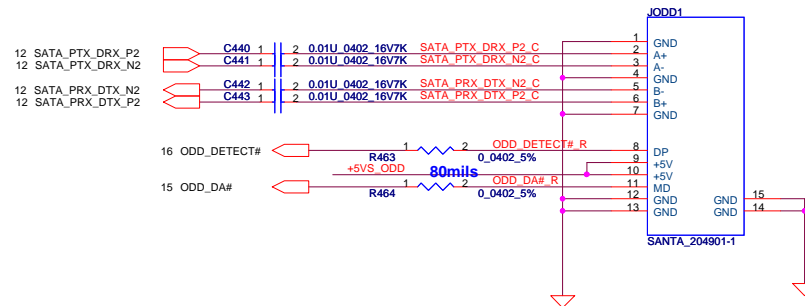


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Date	Thursday, October 27, 2011	Sheet	29	of	59

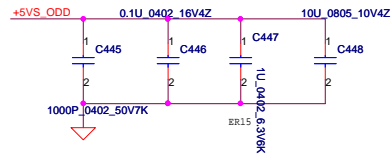
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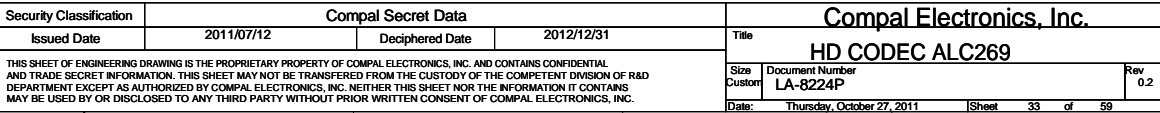
SATA ODD Conn.

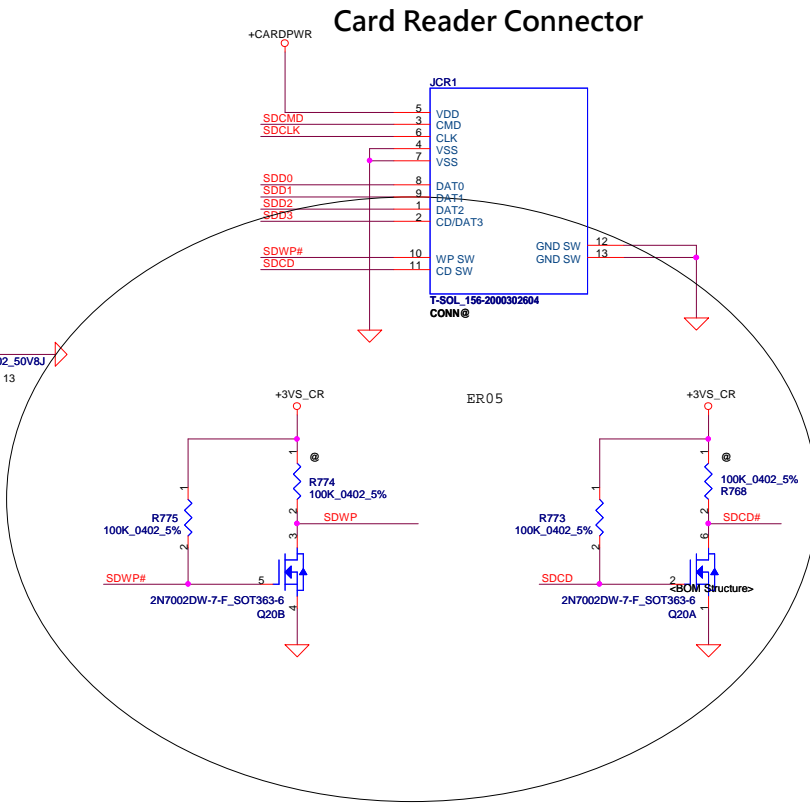
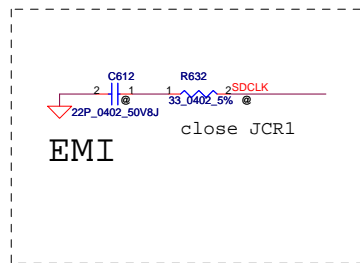
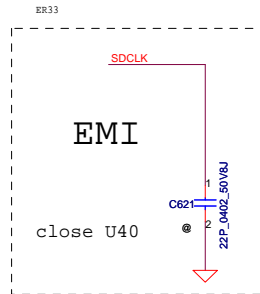
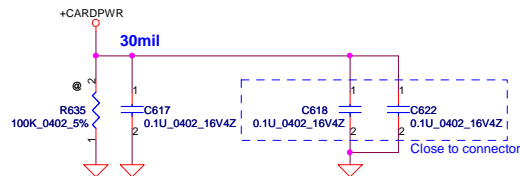
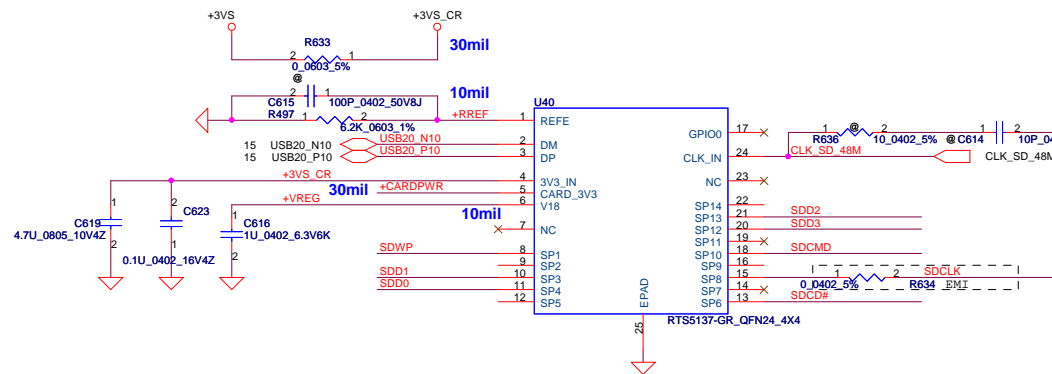


Place caps. near ODD CONN.

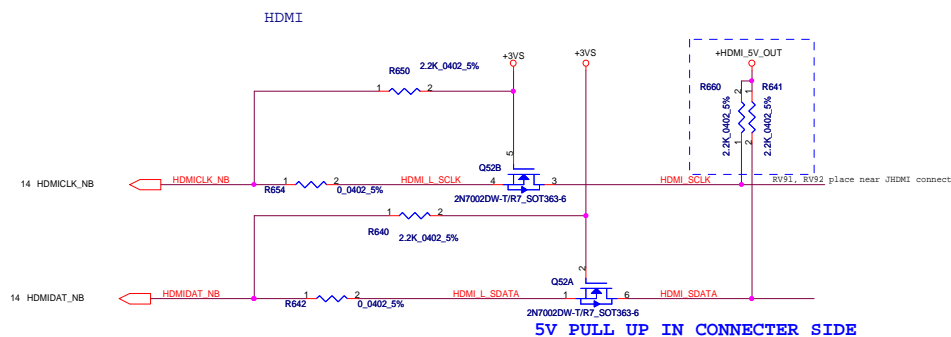
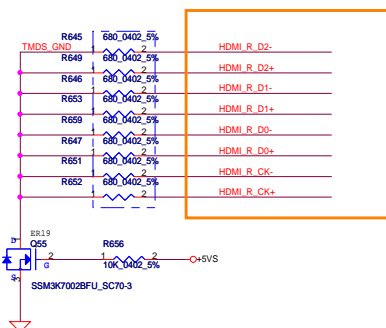
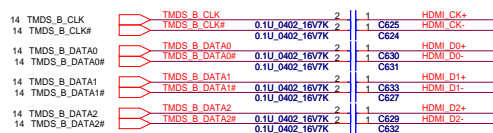
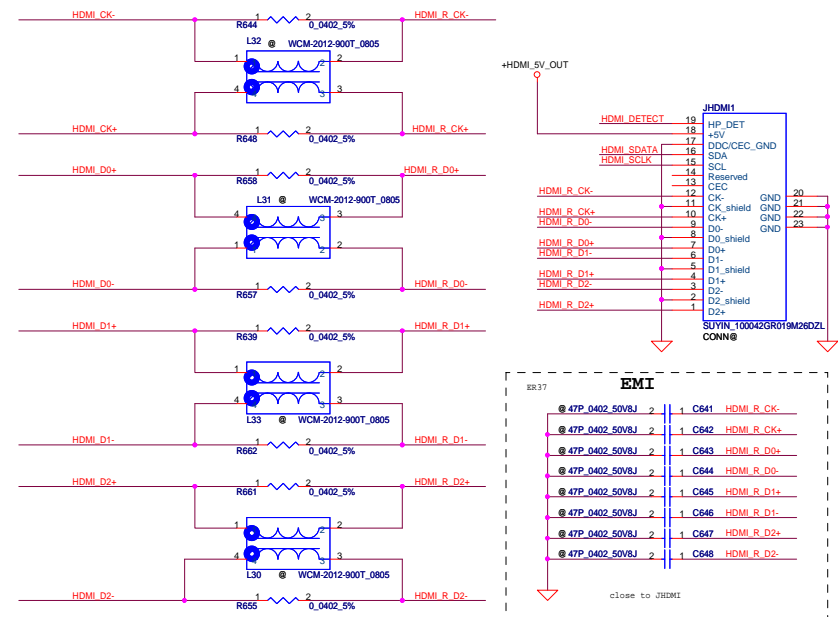
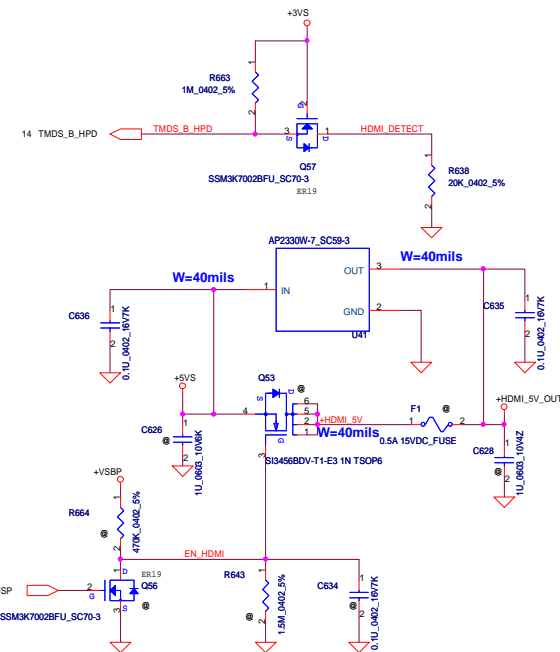
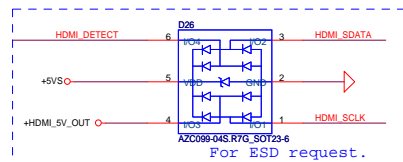


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				HDD & ODD CONN			
				Size B		Document Number	
				LA-8224P			
Date:		Thursday, October 27, 2011		Sheet		31 of 59	





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Date: Thursday, October 27, 2011				Sheet 34 of 59				Size Custom			
Document Number				LA-8224P				Rev			
0.2											



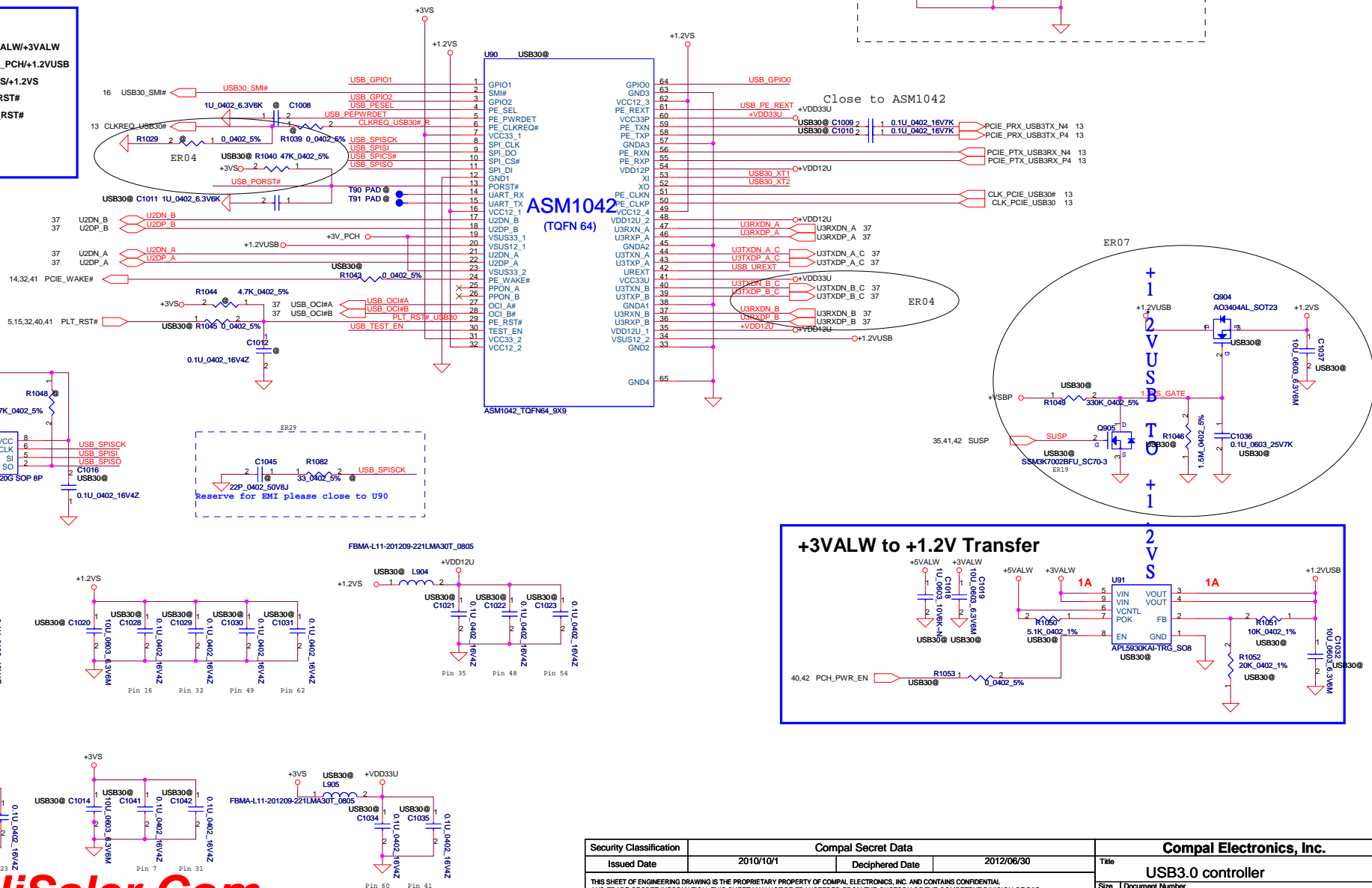
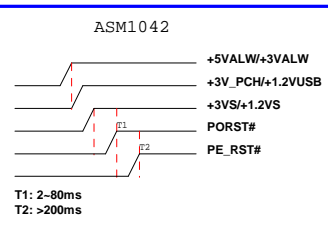
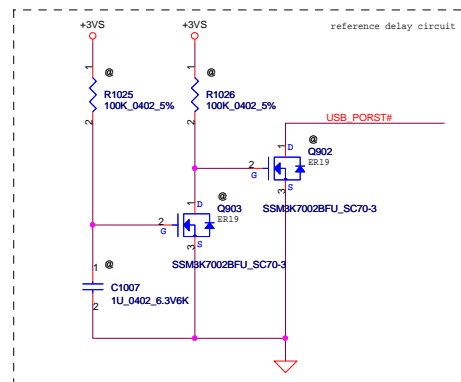
Power Sequence



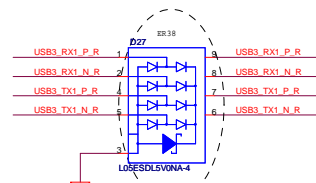
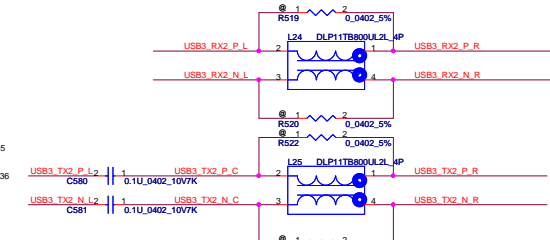
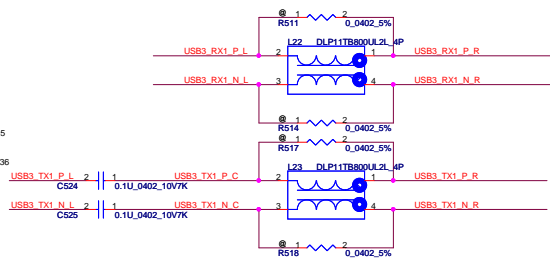
USB_PEPWRDET

USB_PESSEL

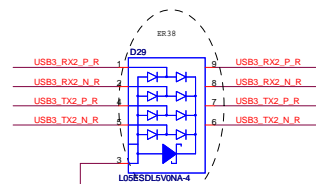
* Other applaction	@
Express Card/Mini Card	Mount



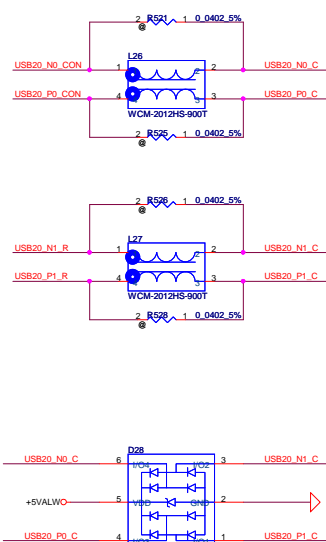
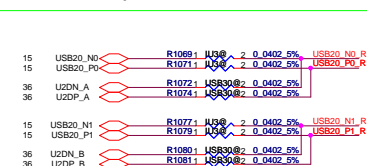
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/10/1	Deciphered Date	2012/06/30	Title		
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				Size	Document Number	Rev
				Custm	LA-8224P	0.2
Date:	Thursday, October 27, 2011	Sheet	36	of	50	



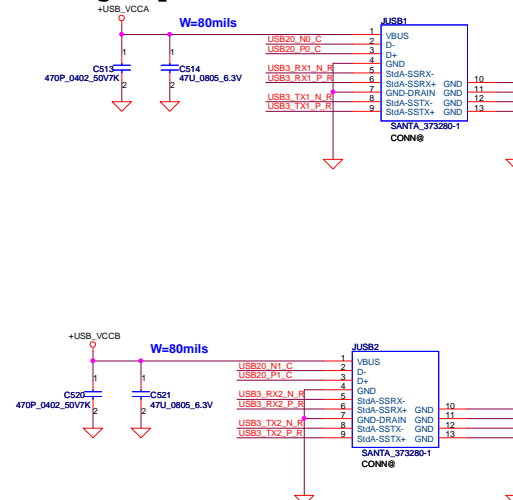
Co-lay USB3.0 (PCH & ASM1042)




Co-lay USB3.0 (PCH & ASM1042)

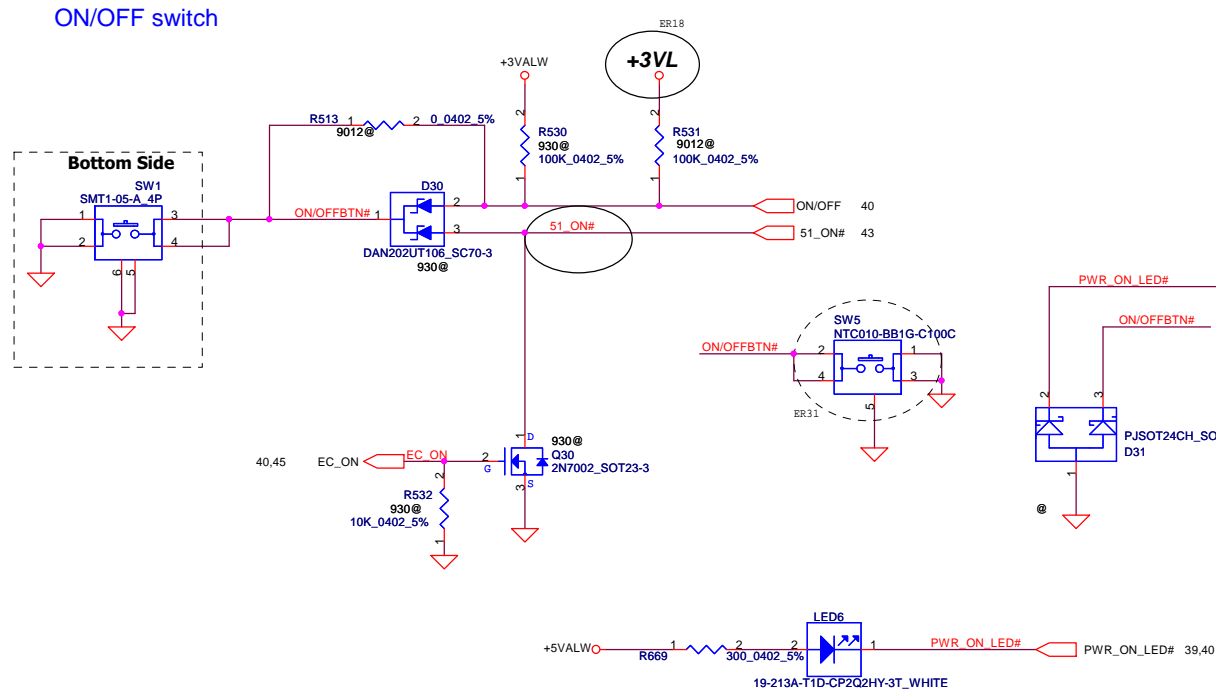


charger port: left side & near user

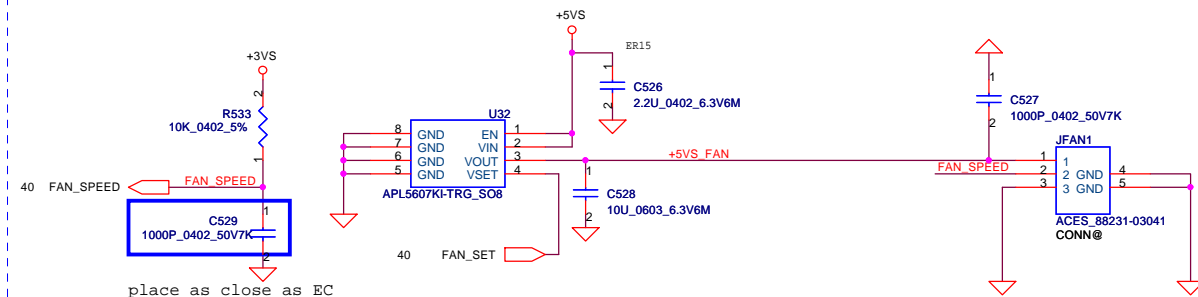


Security Classification		Compal Secret Data			
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	USB2.0/USB3.0 CONN Doc Number: LA-8224P
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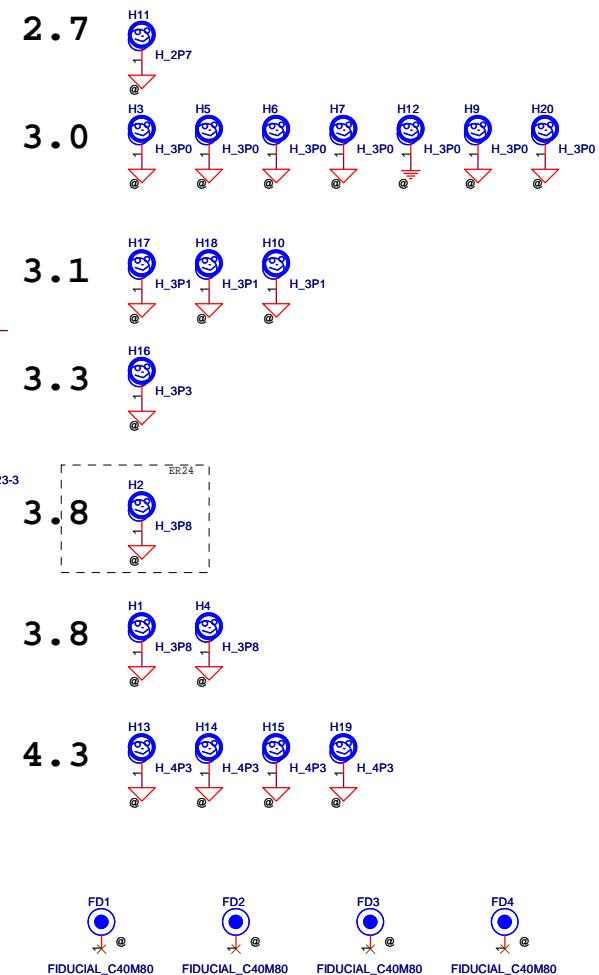
Power Button



Fan Control Circuit

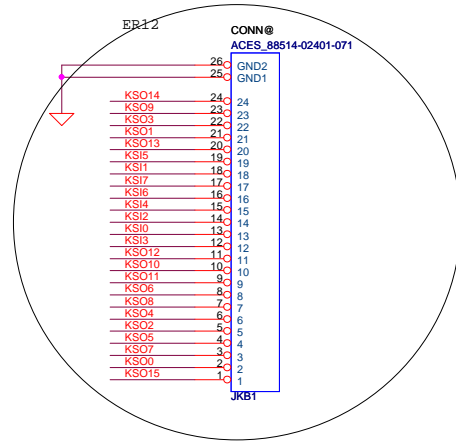
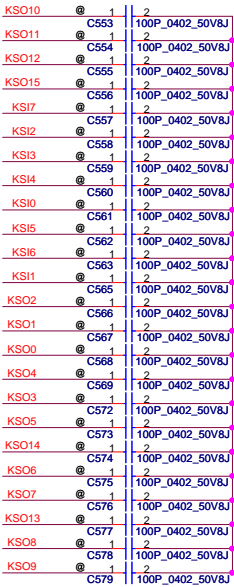
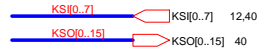


Screw Hole

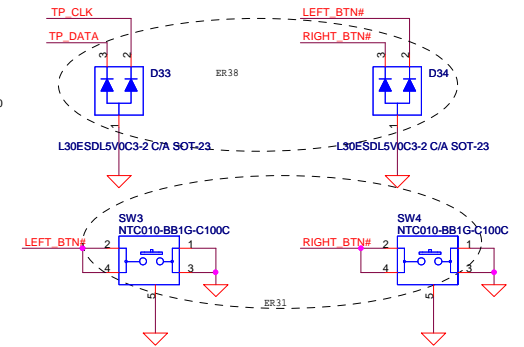
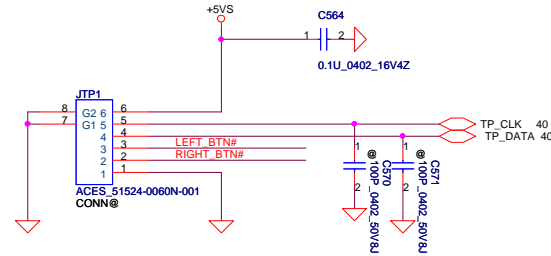


Security Classification		Compal Secret Data		Compal Electronics, Inc. PWRBTN/ FAN / Screws	
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	
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				Document Number LA-8224P	0.2
Date:				Thursday, October 27, 2011	Sheet 38 of 59

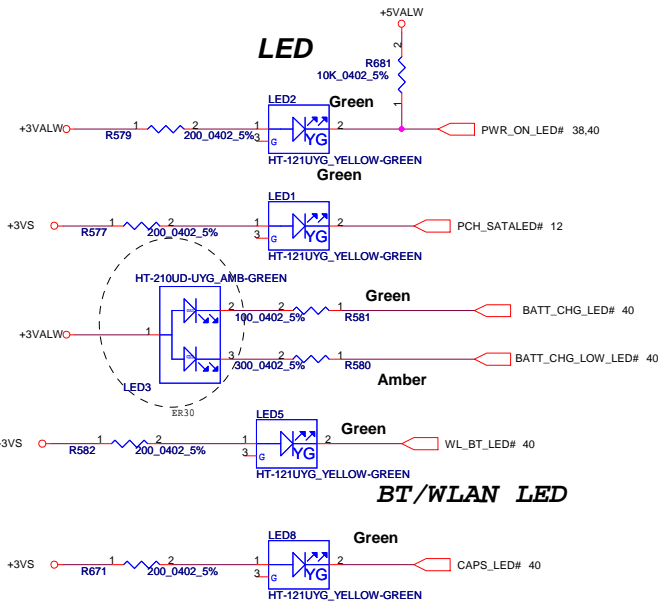
INT_KBD Conn.



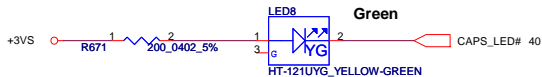
Touch/B Connector



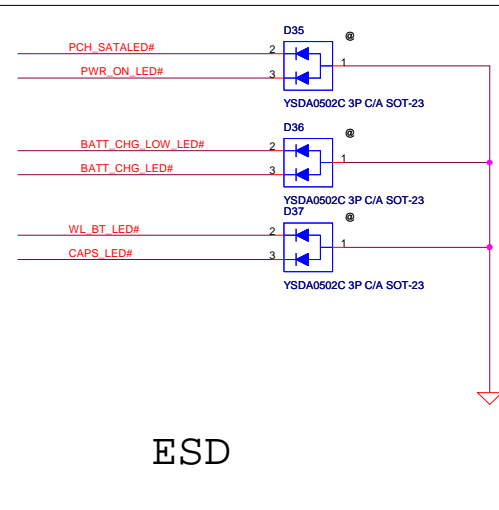
LED



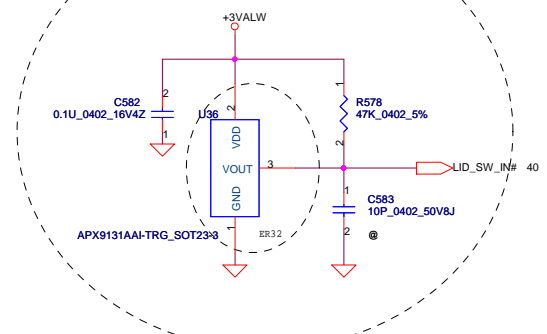
BT/WLAN LED



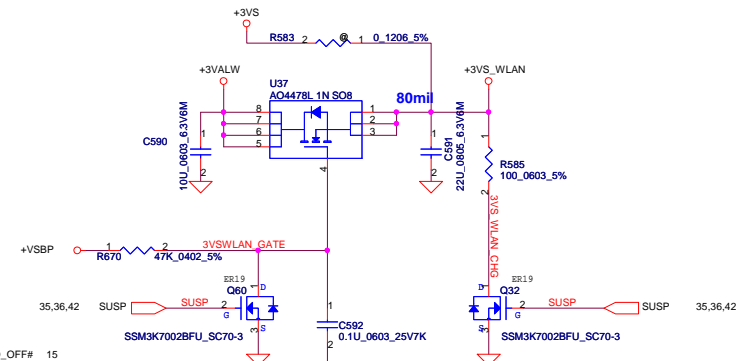
ESD



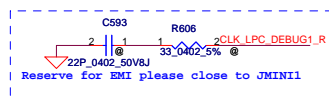
Lid Switch (Hall Effect Switch)



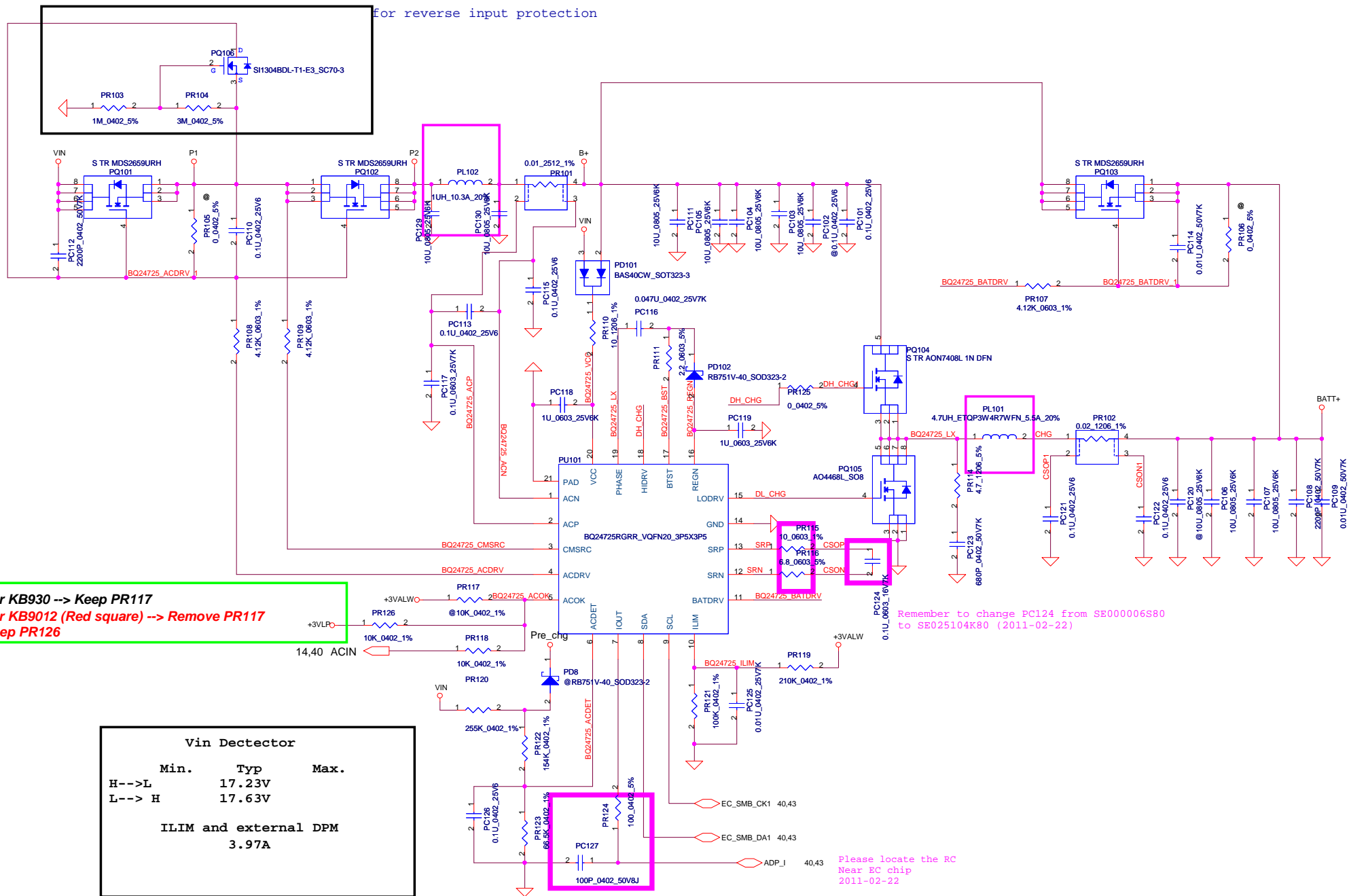
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	KB/EC ROM/TP/FUN/LED
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Rev	0.2
				Date:	Thursday, October 27, 2011
				Sheet	39 of 59

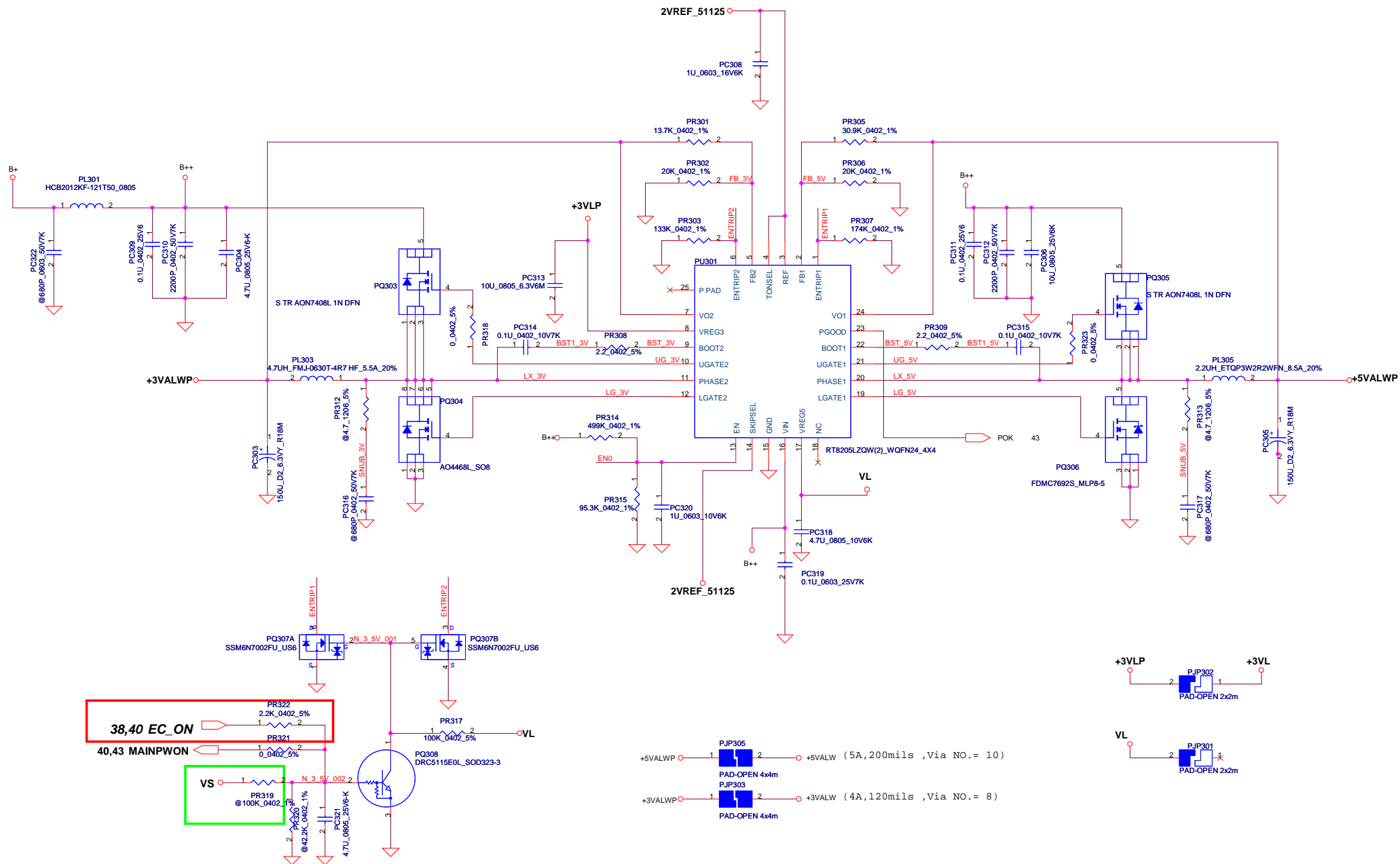


LPC_FRAME#	R599	1	2	0 0402 5% LPC_FRAME#	
LPC_A03# R	R600	1	2	0 0402 5% LPC_A03	LPC_FRAME# 12,40
LPC_A02# R	R601	1	2	0 0402 5% LPC_A02	LPC_A03 12,40
LPC_A01# R	R602	1	2	0 0402 5% LPC_A01	LPC_A02 12,40
LPC_A00# R	R603	1	2	0 0402 5% LPC_A00	LPC_A01 12,40
PLT_RST# R	R604	1	2	0 0402 5% PLT_RST#	LPC_A00 12,40
CLK LPC_DEBUG1	R	1	2	CLK LPC_DEBUG1	CLK_LPC_DEBUG1 15



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					LA-8224P	0.2
Date:				Thursday, October 27, 2011	Sheet	41 of 59





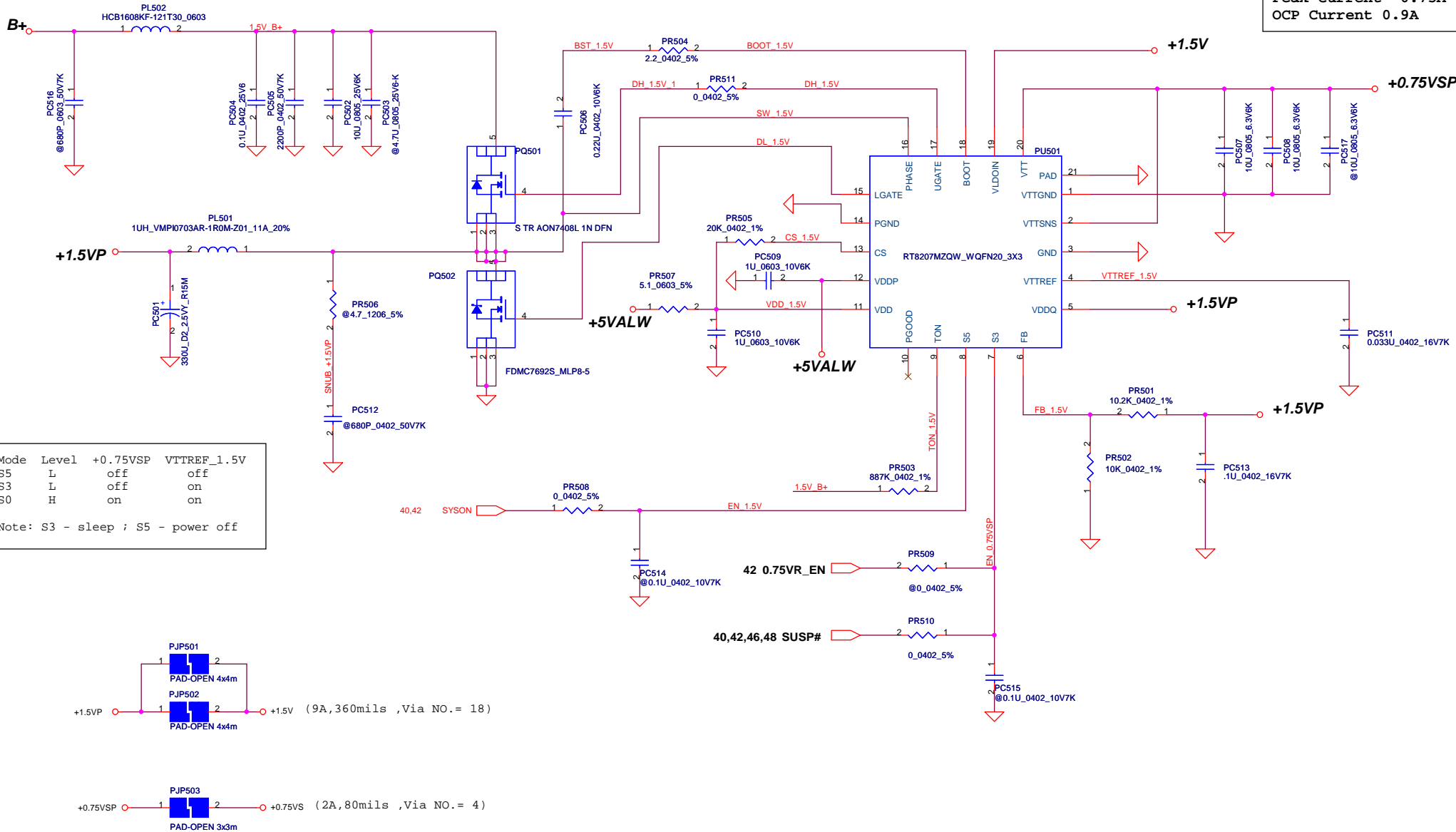
For KB930 --> Keep PR319, Remove PR322
 For KB9012 (Red square) --> Remove PR319
 Keep PR322

Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Size	Document Number
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Date: Thursday, October 27, 2011				Sheet	45 of 59

(8.5A,360mils ,Via NO.= 17)

PJP606,PJP607先斷開,確定拿掉PU605再接上

Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2012/12/31	PWR-V1.05S VCCP	
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				Custom	PBL22 LA-7391P M/B
				Date:	Thursday, October 27, 2011
				Sheet	47 of 59
				Rev	0.2



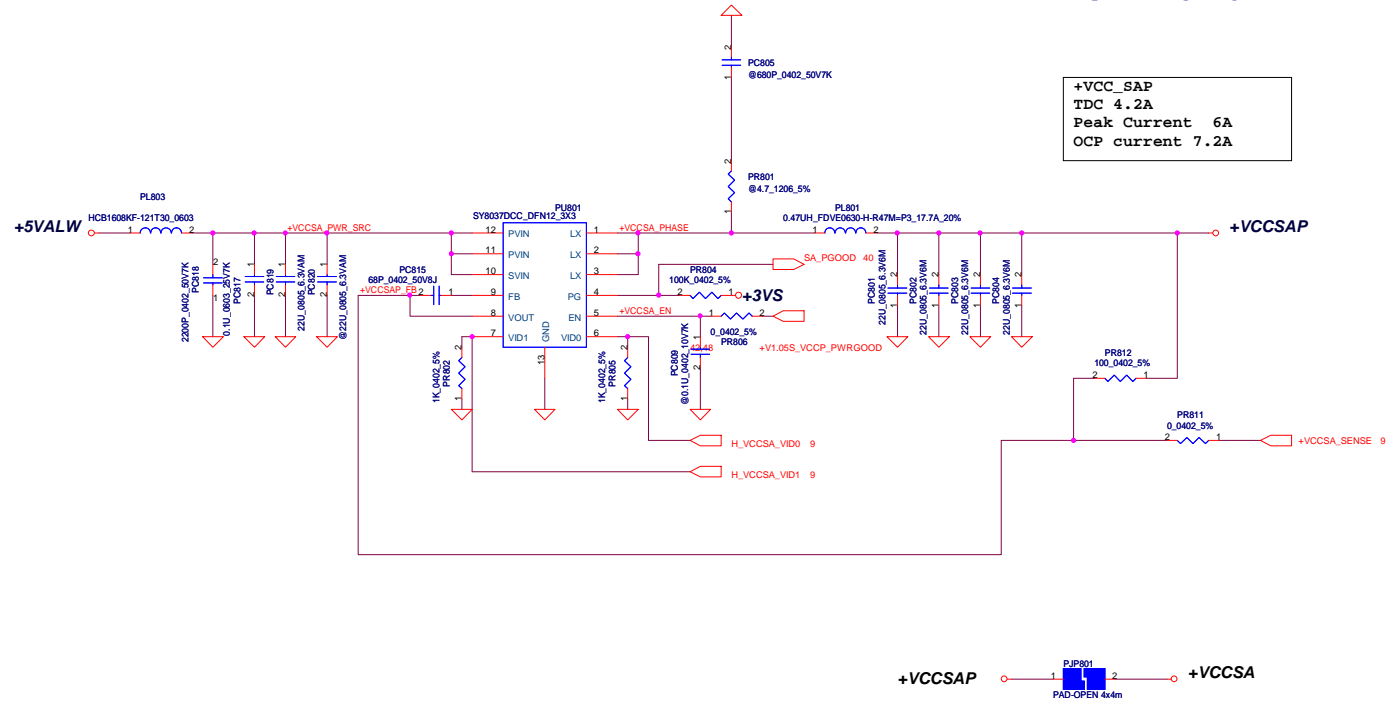
0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

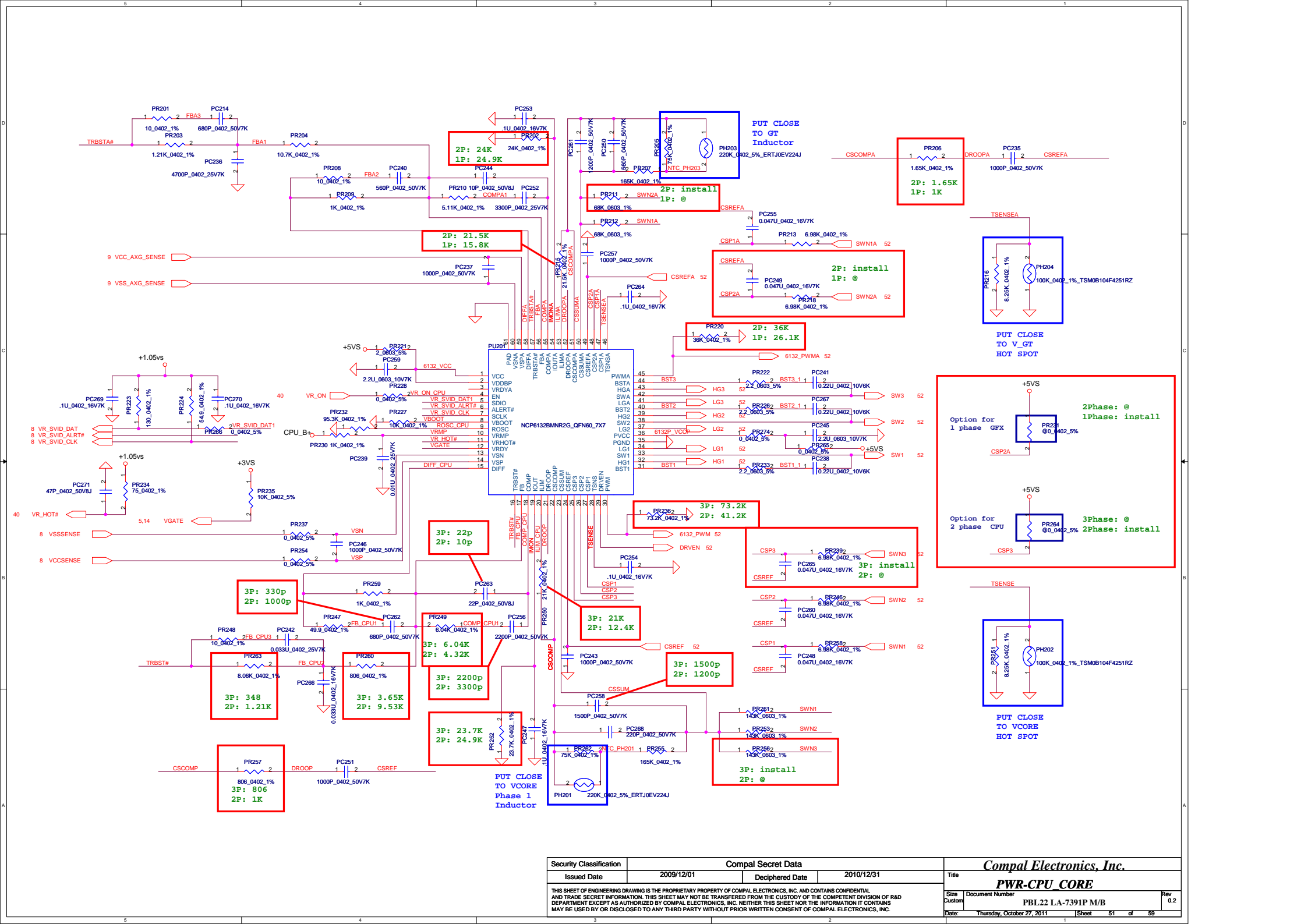
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

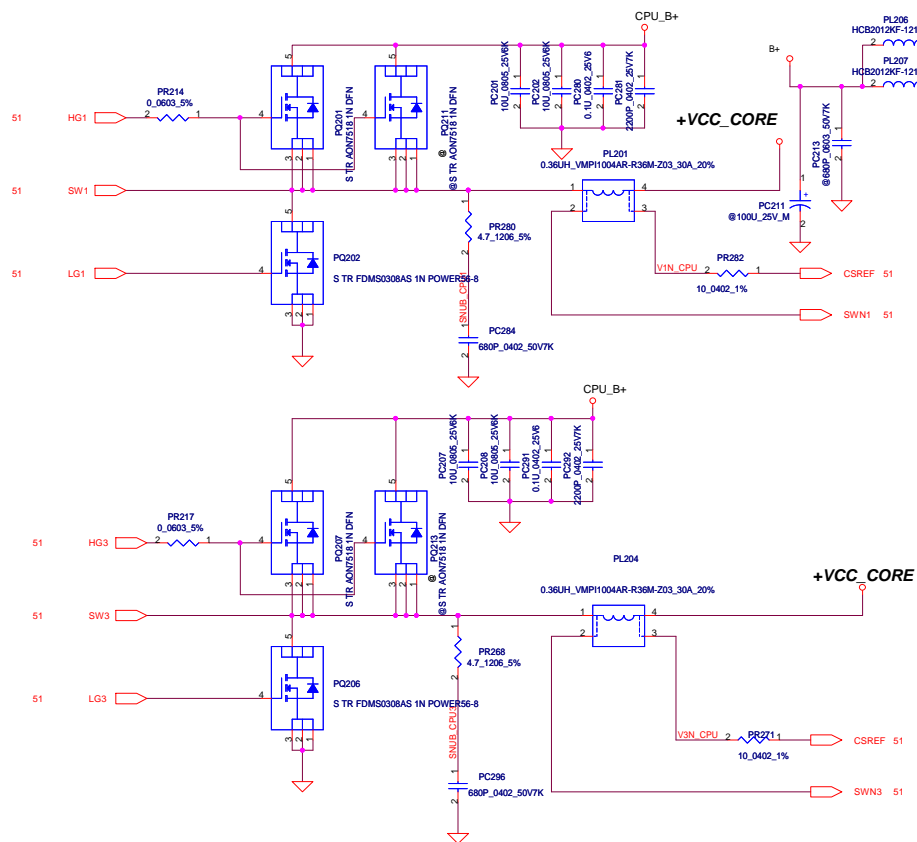
output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



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Size	C	Document Number	PBL22 LA-7391P M/B	Rev
Date	Thursday, October 27, 2011	Sheet	50	of 59



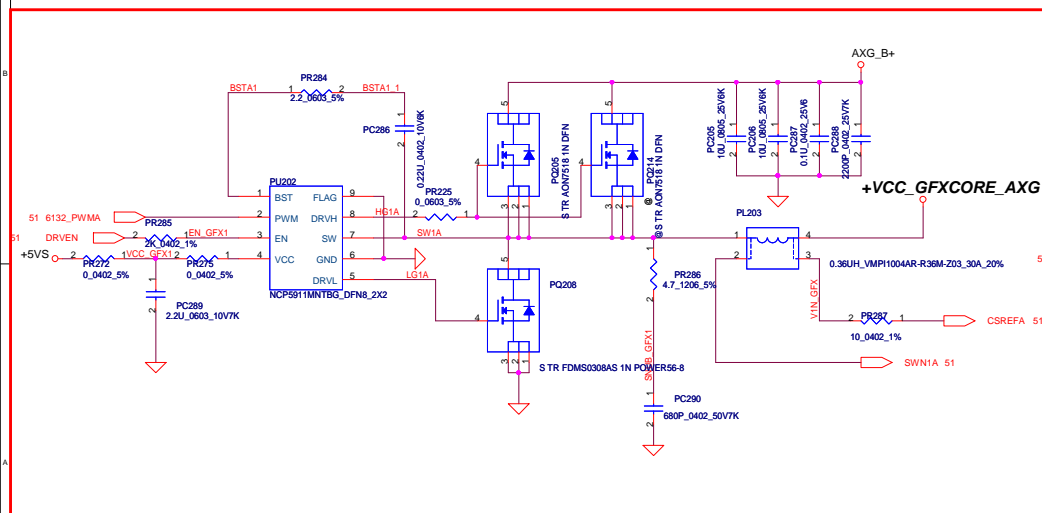


QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=56A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=33A
R_LL=1.9m ohm
OCP~65A

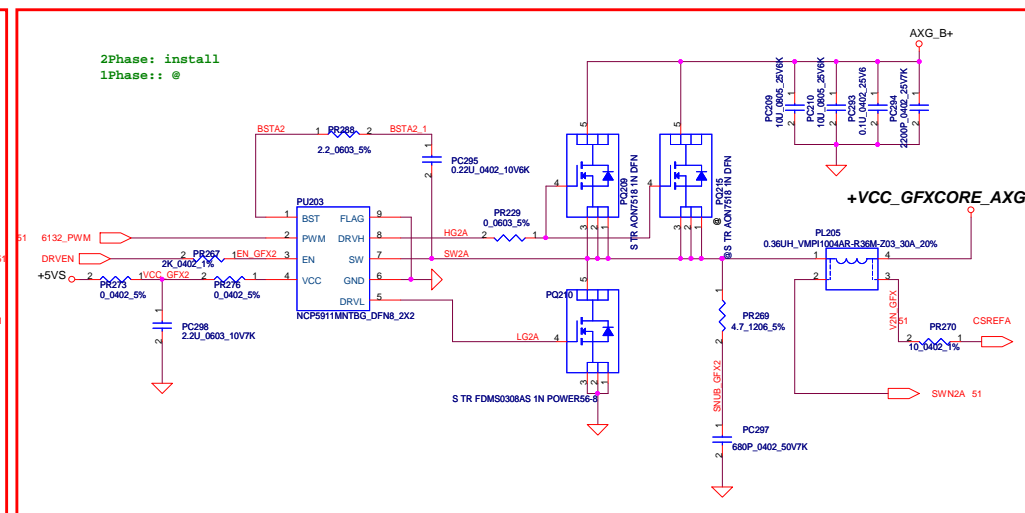
QC 45W CPU
solution: 3+2
MOS: cpu_core --> 上1(CSD17308) 下1(TPCA8059)
Gfx_core --> 上1(CSD17308) 下1(TPCA8059)

DC 35W CPU
solution: 2+1
MOS: cpu_core --> 上1(CSD17308) 下1(TPCA8059)
Gfx_core --> 上1(CSD17308) 下1(TPCA8057)

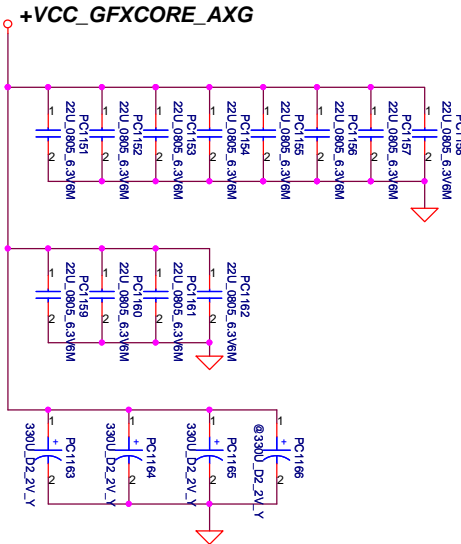
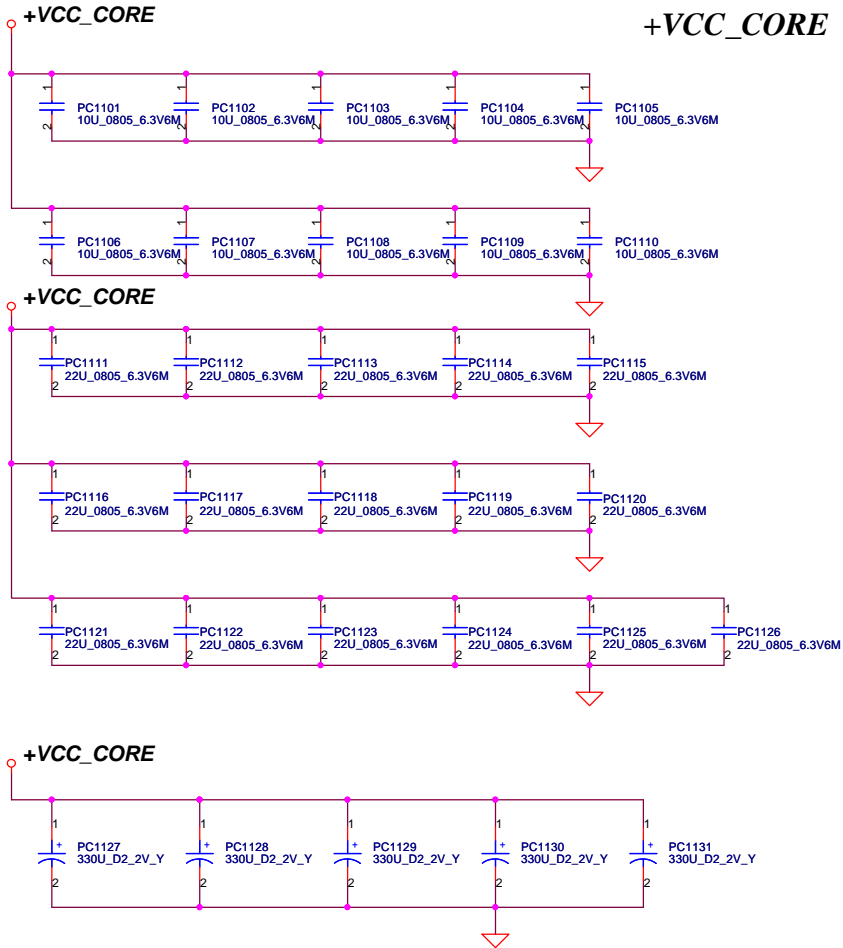


QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

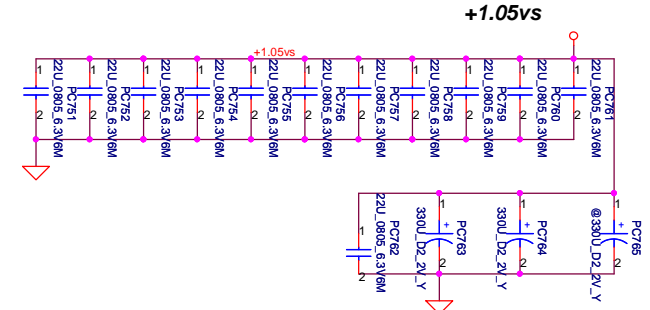


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Issued Date		Deciphered Date		Title	
2009/12/01		2010/12/31		PWR-CPU CORE	
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		C		PBL22 LA-7391P M/B	
		Date		Thursday, October 27, 2011	
		Sheet		52 of 59	



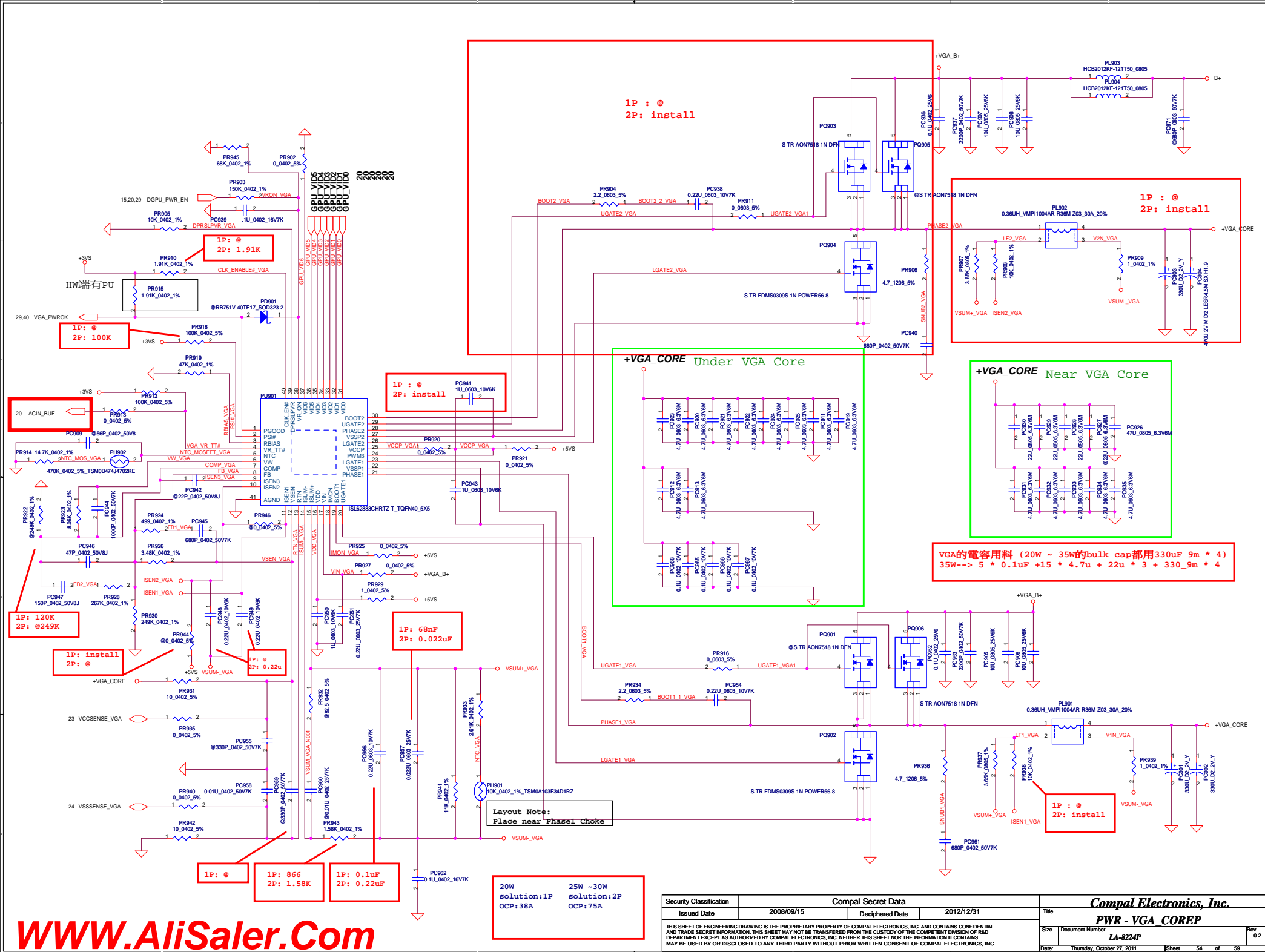
Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

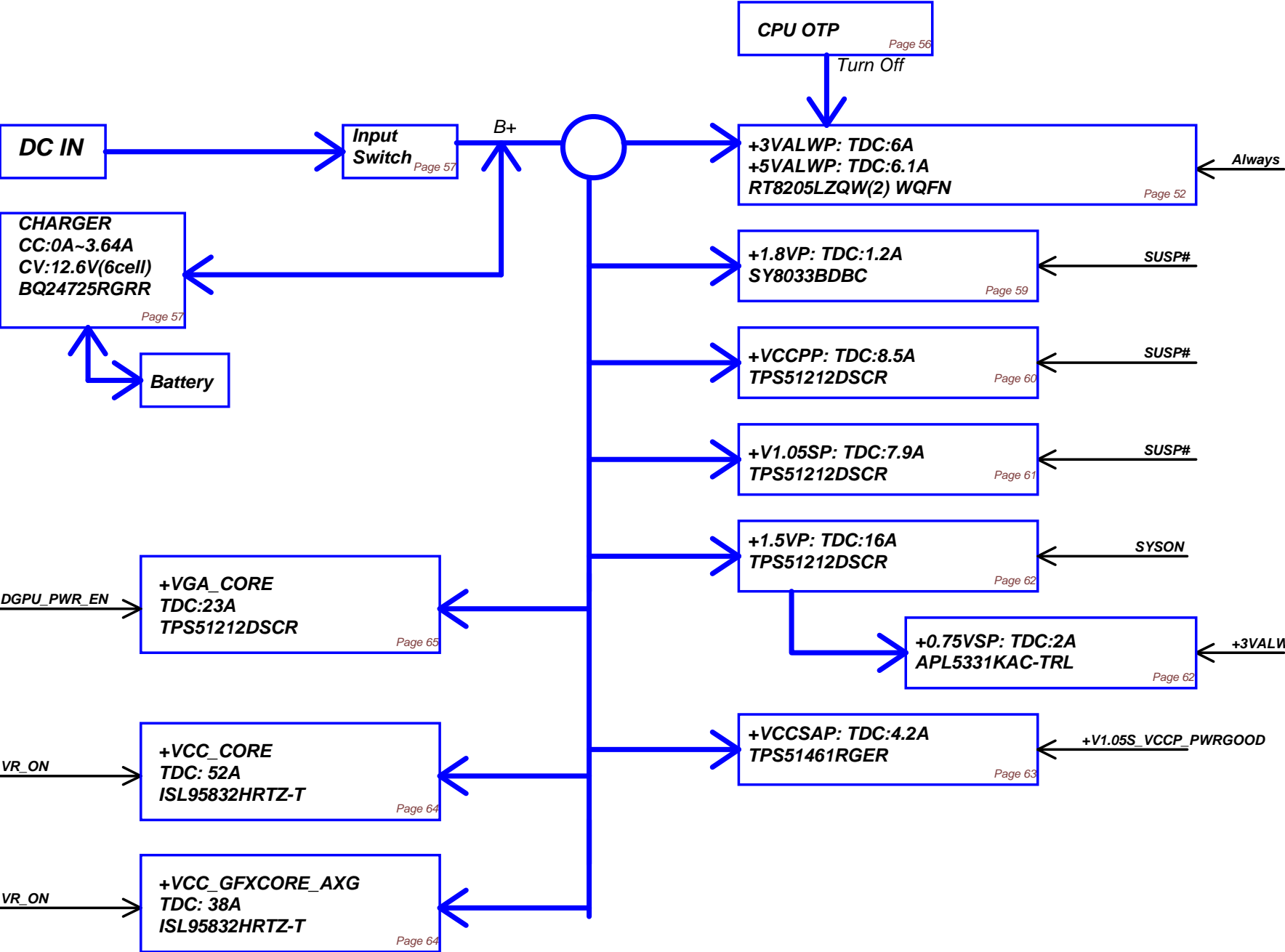
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2012/12/31	Title	PWR - PROCESSOR DECOUPLING
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				Date	Thursday, October 27, 2011
				Sheet	53 of 59
				Rev	0.2



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Title		Compal Electronics, Inc.	
Size		PWR - VGA CORE	
Document Number		LA-8224P	
Date		Thursday, October 27, 2011	
Sheet		54 of 59	

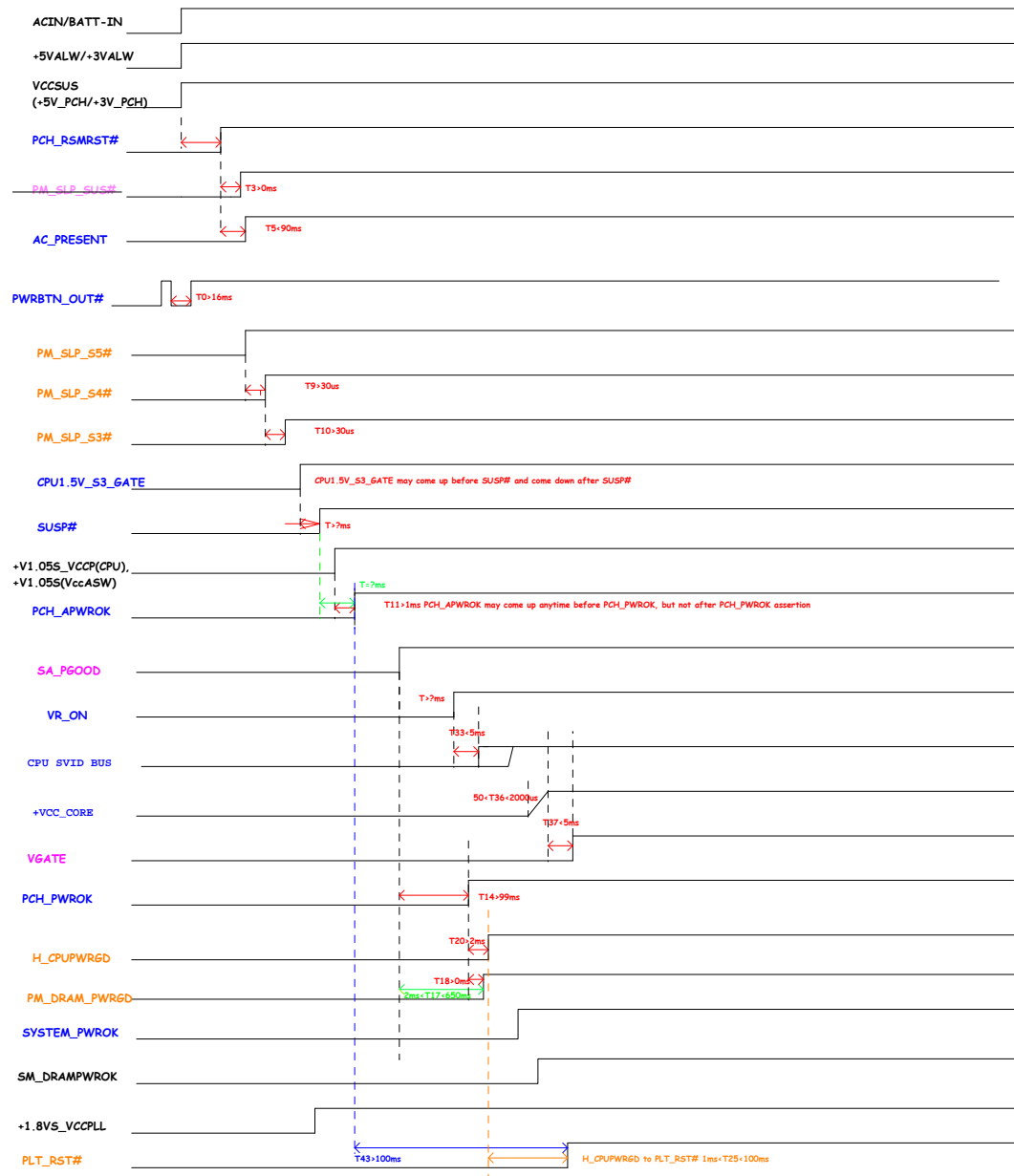
Power block



Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Security Classification		Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2012/12/31	PWR - PIR	
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					LA-8224P
Date: Thursday, October 27, 2011				Sheet	56 of 59

Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		HW Design (TMDS_B_HPD)	0.2	14	Delete R205	09/21	
ER02		For non AI co-lay	0.2	37	Add R745,R746 for non AI	09/21	
ER03	+3VS Leakage	HW Design (SMBus leakage)	0.2	13	AI parts change to AI@	09/21	
ER04	Can't detect USB30 (JUSB2)	HW Design (PCB2)	0.2	40	Delete Q3. (connect pin S & D) remove R135, R137	09/21	
ER05		Design change for card reader	0.2	34	Del R552, R556	09/21	
ER06		HW Design (PURC demand)	0.2	29	Swap U90,39/40 to U90,36/37 net	09/21	
ER07		HW Design(PCB2)	0.2	36	Change R1040 to 47K from 4.7K ohm	09/21	
ER08		HW Design (PURC demand)	0.2	42	Reserve R1029	09/21	
ER09		Fine-tune GPU timing	0.2	29	Add Q20, R773, R775	09/22	
ER10		HW Design (reserve)	0.2	18	Reserve R768, R774	09/22	
ER11		HW Design(PCB2) for add VRAM DDR3 512MX8	0.2	25,26,27,28	Change Net name at Card reader Conn	09/21	
ER12		HW Design (change)	0.2	39	Change to Q3(A03404L) from U22(A04430L)	09/21	
ER13		HW Design	0.2	40	Change R1049 to 330k	09/21	
ER14		HW Design (PURC demand)	0.2	15	Change Q904 to A03404L from AP2301GN	09/21	
ER15		HW Design (PURC demand)	0.2	29,31,37,38,10,11	Change R1046 to 1.5M	09/21	
ER16		HW Design(XTAL fine-tune)	0.2	42,12,13,32,20,36	Change Q33 to A03413L from AP2301GN	09/21	
ER17		HW Design for instant on function	0.2	13	Change R433 to 0 ohm un-stuff C396	09/21	
ER18		HW Design (power jumper change to +3VL)	0.2	38	Change R432 to 10K	09/21	
ER19		HW Design (PURC demand)	0.2	40	Change R435 to 200 ohm	09/21	
ER20		EMI solution	0.2	5	Reserve R290	09/21	
ER21		Refer to ORB design	0.2	14	Add CMDA14 signal (U12-U19 pin J7)	09/28	
ER22		change for GPU H/W strapping STRAP1 to PL 45K ohm to enhanced the PCIe PEG driving.	0.2	22	Reverse JKB1 connector	09/30	
			0.2	40	Del Y5 , C545 , C546	09/30	
			0.2	15	Del R229,R230 (10K) Add R776-R783 (10K)	09/30	
			0.2	29,31,37,38,10,11	Del R237,R239,R242 (8.2K) Add R784-R793 (8.2K)	09/30	
			0.2	42,12,13,32,20,36	Change P/N C387,C389,C399,C436,C447,C602	10/03	
			0.2	13,32,20,36	Change P/N C509,C515,C518,C526,(0402)	10/03	
			0.2	13,32,20,36	Change P/N C99,C109,C118,C120,C140,C141.(0402)	10/03	
			0.2	13,32,20,36	Change R607 to 10 ohm Change Y3,C900,C901.	10/07	
			0.2	13,32,20,36	Change Y1,C144,C145 Change Y4,C469,C473.	10/07	
			0.2	13,32,20,36	Change Y2,C163,C164 Change Y9	10/07	
			0.2	13,32,20,36	Reserve R750	10/07	
			0.2	13,32,20,36	R576 pin2 change to +3V_PCH from +3VS	10/07	
			0.2	13,32,20,36	Change R576 to 0	10/07	
			0.2	40	jumper PJP302 (change +3VLP to +3VL @P38,P40)	10/07	
			0.2		Change P/N Q7,U20,U21.	10/14	
			0.2		Change P/N Q14-Q19,Q25,Q27-Q29,Q32,Q34-Q37,Q40-Q43, Q46-Q51,Q55-Q57,Q60,Q61,Q902,Q903,Q905.	10/14	
			0.2		Change P/N Q23	10/14	
			0.2	5	Add R684 to 0 (H_CPUPWRGD)	10/14	
			0.2	14	un-stuff D2, Add R751	10/14	
			0.2	40	un-stuff D32, R547, Add R752	10/14	
			0.2		Assign U33.18 to AC_PRESENT signal.	10/14	
			0.2	22	Change R349 from 34.8K to 45.3K	10/14	

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				Date:	Thursday, October 27, 2011
				Sheet	58 of 59
				Rev	0.2

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER23		modify parts for Intel review feedback message.	0.2	09 18 17 14 15	Add R289 , Add C149 0.1uf Del L6, Add R289 , un-stuff C212 Del L4, Add R387 Add R230 Stuff R244	10/14	
ER24		Modify H2 size	0.2	38	Modify H2 size	10/17	
ER25		Refer to Intel review feedback item 45.	0.2	16	Add R807	10/19	
ER26		Reserve for Deep Sx	0.2	14,16 40	Add unstuff R800,R801,R802,R803,R804,R805 Add PCH_DPWROK,DS_WAKE#,SUSACK#,SUSWARN#	10/19	
ER27		Reserve for ROM protect	0.2	40	Add unstuff R806	10/19	
ER28		For Instant On function control by EC	0.2	06	Stuff R44, Unstuff R43	10/19	
ER29		RF request	0.2	36	Reserve R1082 , C1045	10/19	
ER30		For LED issue	0.2	39	change LED3 footprint to LED_HT-210UD-UYG_3P	10/20	
ER31		PRUC request	0.2	38 39	Change SW3,SW4,SW5 P/N	10/20	
ER32		PRUC request	0.2	39	Change U36 P/N	10/20	
ER33		For EMI request (without MS_CLK)	0.2	34	Remove R637,C611,R631,C620.	10/20	
ER34		dGPU thermal throttling.	0.2	20 40	Add R428, Revise U11 I/O signal. Un-stuff R730.	10/20	
ER35		SPI flash data crisis prevention.	0.2	12 40	Add Q63, R135, R137. Change U33.41 net to EC_SPI_WP. remove R806.	10/20	
ER36		Power switch EOS issue prevention.	0.2	37	Change C510, C516, C519 to 0.22uF/16V.	10/20	
ER37		For EMI request	0.2	32 35	Change R485 , R486 to 0.1uF Reserve C641~C648	10/20	
ER38		For ESD request	0.2	37,35 30,39	Change D27,D29,D24,D25. Change D6,D7,D9,D10,D33,D34.	10/20	
ER39		Modify X76 table (N13P-GS & N13M-GE1 x8)	0.2	3	update X76 table (add ZZZ9 ~ZZZ12 for N13P-GS & N13M-GE1 x8) & P/N	10/25	
ER40		update Power circuit	0.2	43~56	update Power circuit. (PC211)	10/26	
ER41		Modify PCH_SPI_WP# singal control by EC	0.2	12	Stuff R135	10/26	
ER42		Add test point for DFT	0.2	20	Add GPU_JTAG_TCK,GPU_JTAG_TDI,GPU_JTAG_TDO, GPU_JTAG_TMS	10/27	
ER43		For ASM1042 OC# pull-up	0.2	37	Reserve R1023,R1024 un-stuff	10/27 b	

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					Date:	Friday, October 28, 2011	Sheet 59 of 59